Welcome To

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Session 25
High-Bandwidth Low-Power DRAM and I/O

A 3.2Gbps/pin 8Gbit 1.0V LPDDR4 SDRAM with integrated ECC engine for sub-1V DRAM core operation

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Outline

- LPDDR4 Key Features
- Top Chip Structure
- Circuit Implementation
- Measurement Result
- Chip Summary
- Conclusion

LPDDR4 Key Features

	LPDDR3	LPDDR4
Pin Speed	Max. 2133Mbps	Max. 4266Mbps (3200Mbps in this Work)
I/O Interface	HSUL_12	LVSTL_11
Termination	N/A	40ohm VSSQ Term.
DBI	N/A	DC DBI
Burst Length	8	16, 32
No. of Channel	1Ch. per Die	2Ch. per Die
Number of IO's	x32 I/O	X16 I/O per Ch.
Supply Voltage	1.2V	1.1V (1.0V in this Work)

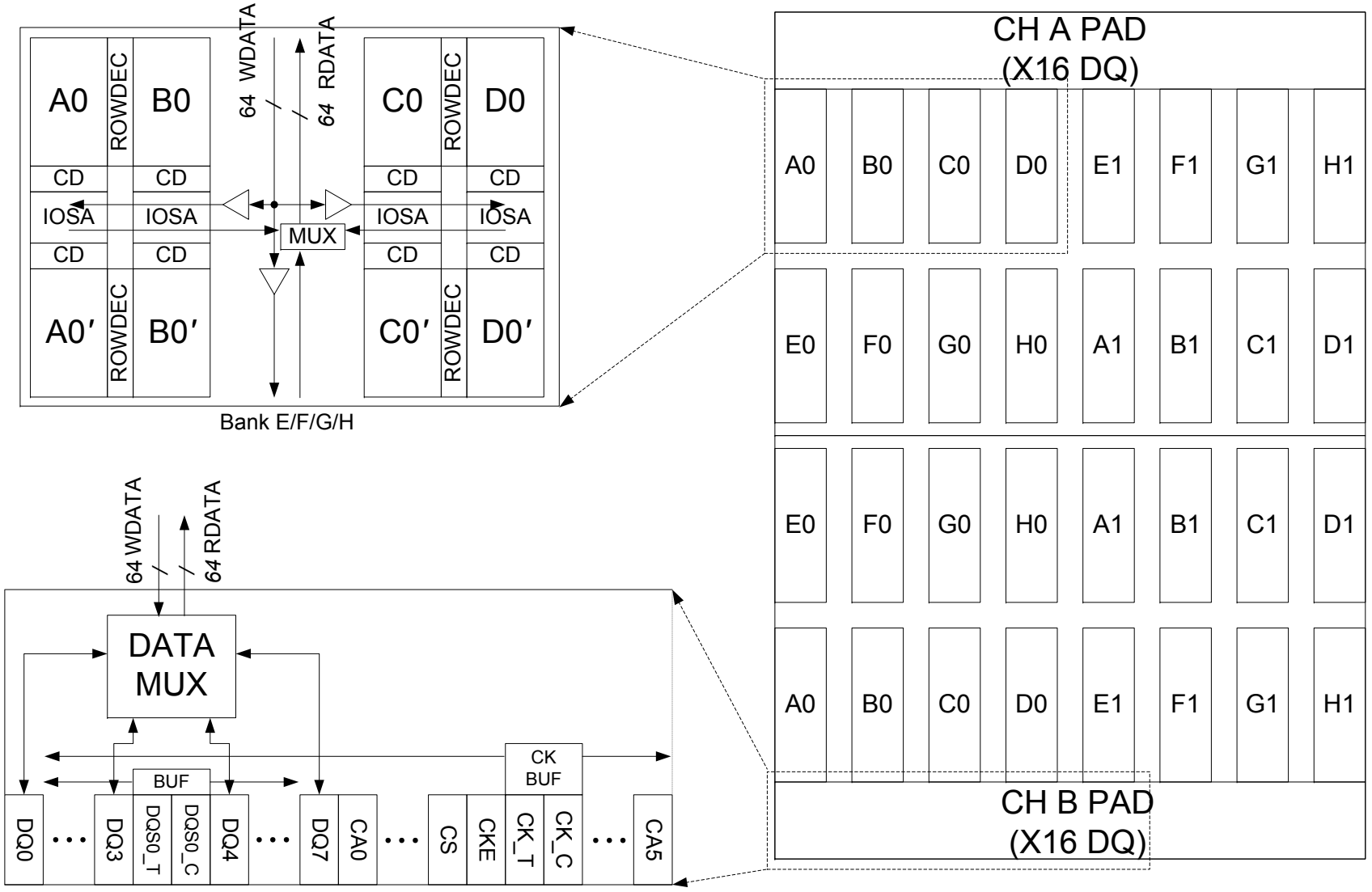
LPDDR4 Architecture

- 2 Independent channels with X16 DQ.
  - Approx. 15% current consumption reduction achieved by shorter datapath and clock tree.

- 16n prefetch core.
  - 200MHz core cycle @ 3200Mbps operation
  - 16(BL)X16(DQ) = 256bit data access granularity.

- 1:8 SERDES in DQ IO.
  - Additional 1:2 SERDES in IO sense Amp. area for 16n prefetch structure.

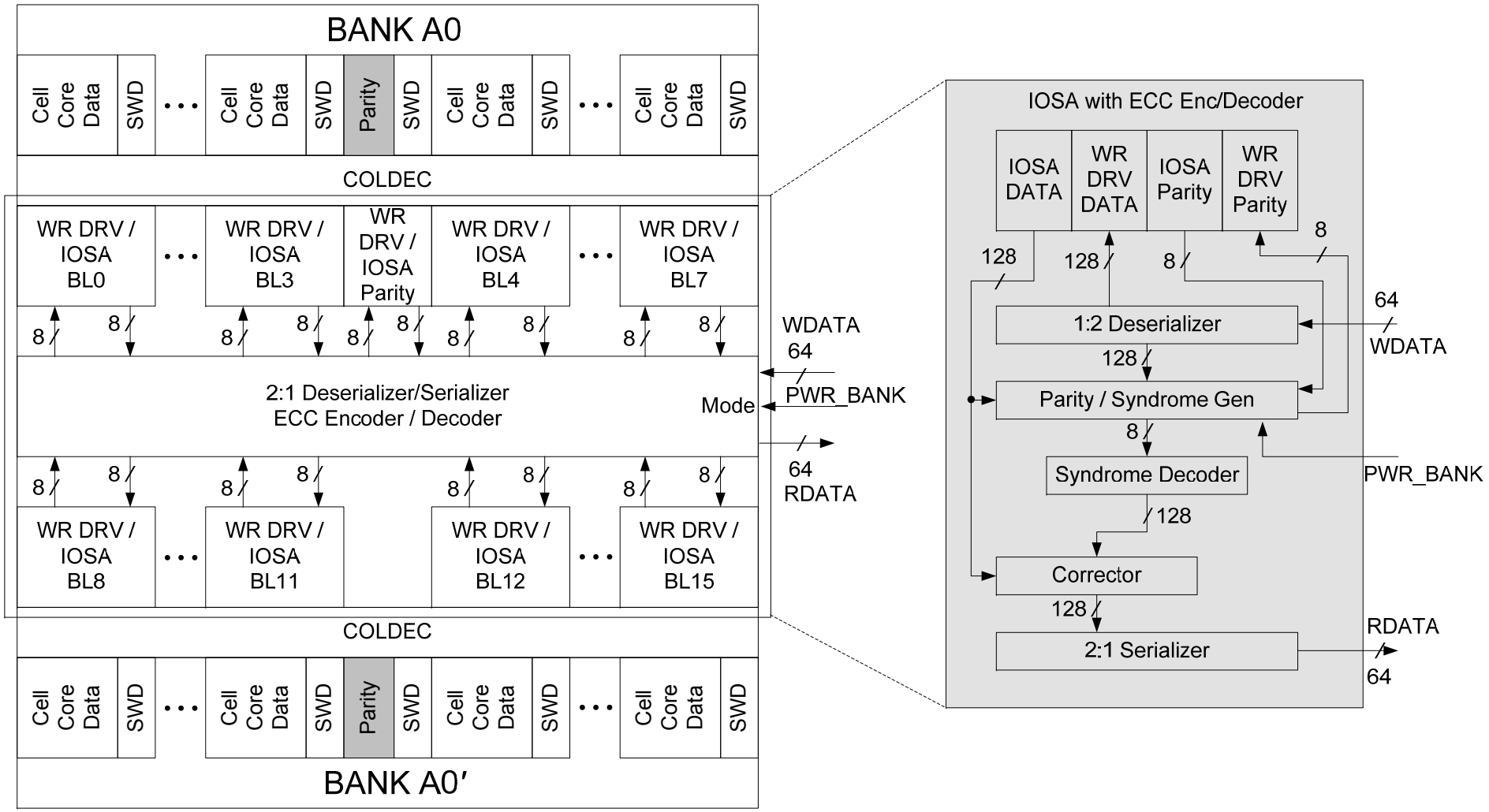
Top Chip Structure



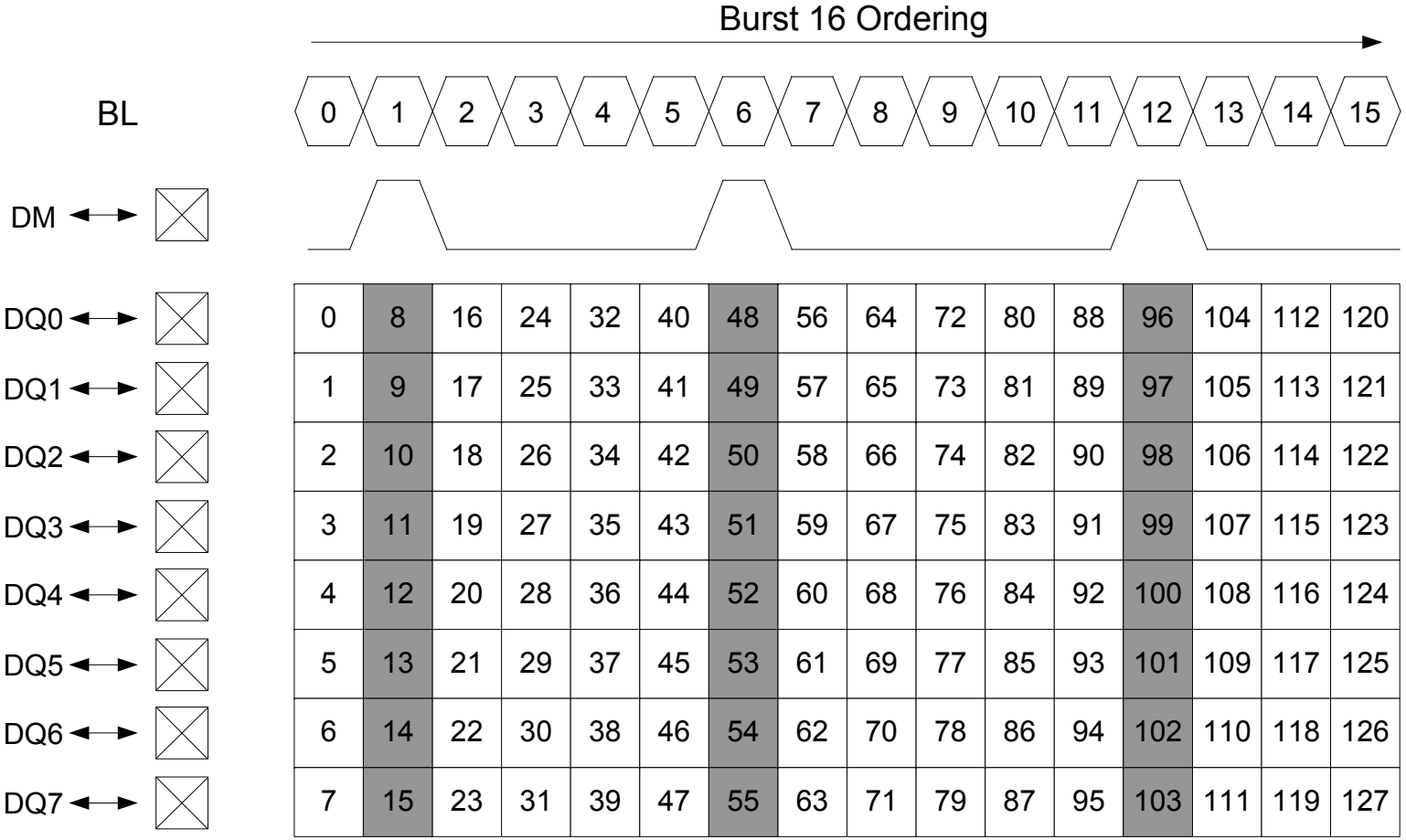
Integrated ECC

- 1V power supply
  - Number of fail bits are increased to unrepairable level by redundancy only.
- (136,128) Shortened hamming code
  - Single error correction capability.
- Each bank has own ECC encoding/decoding engine
  - Minimized additional timing constraints occurring from error correction operation.
- Shared circuit for parity and syndrome generator
  - Reduced die overhead from ECC engine.

ECC Encoder/Decoder



Data Masked Write



0	8	16	24	32	40	48	56	64	72	80	88	96	104	112	120
1	9	17	25	33	41	49	57	65	73	81	89	97	105	113	121
2	10	18	26	34	42	50	58	66	74	82	90	98	106	114	122
3	11	19	27	35	43	51	59	67	75	83	91	99	107	115	123
4	12	20	28	36	44	52	60	68	76	84	92	100	108	116	124
5	13	21	29	37	45	53	61	69	77	85	93	101	109	117	125
6	14	22	30	38	46	54	62	70	78	86	94	102	110	118	126
7	15	23	31	39	47	55	63	71	79	87	95	103	111	119	127

: Masked Data (Existing cell data should not be overwritten by masked data.)

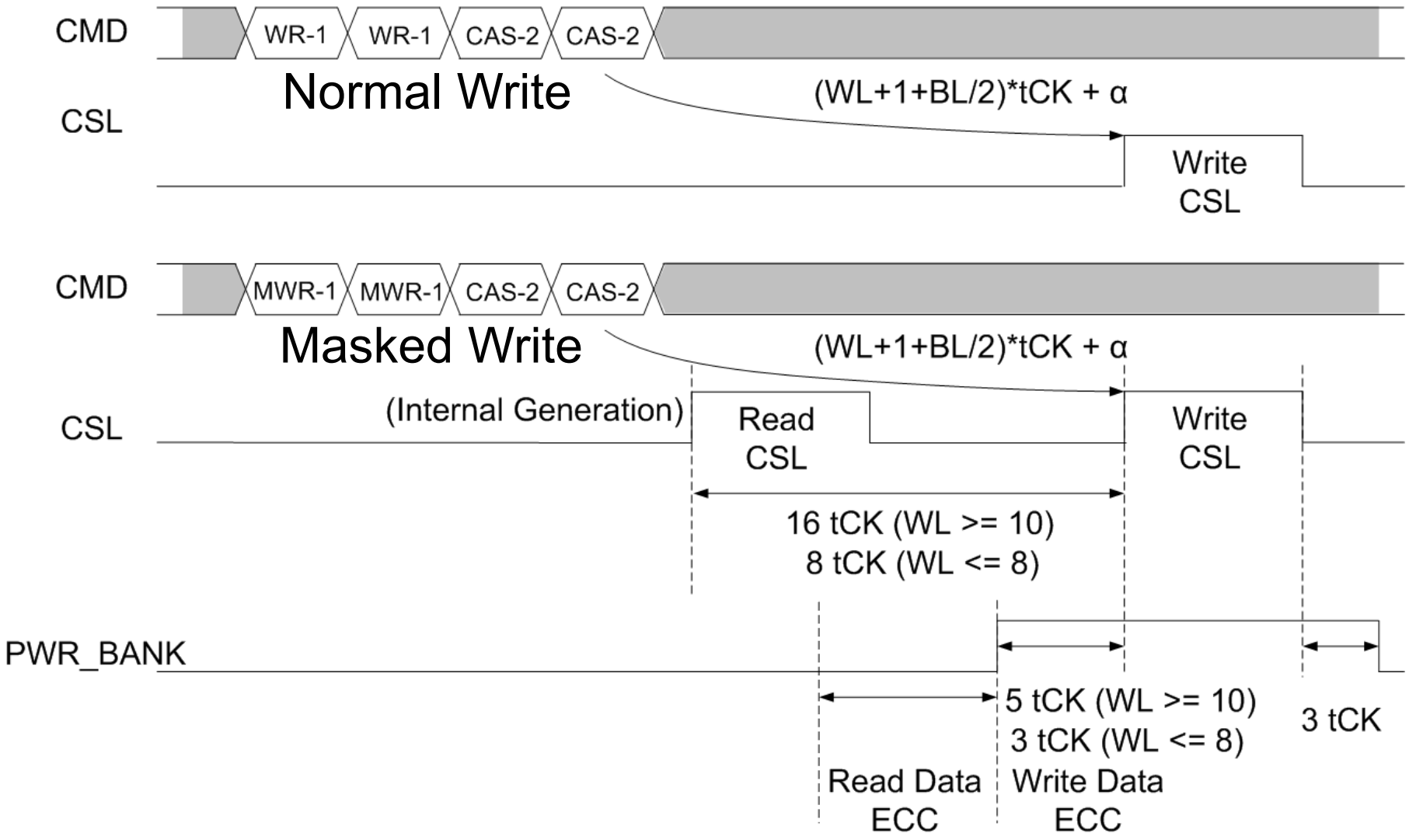
- In conventional DRAM, ECC parity generation is impossible because only part of message data is available in data masked write operation.

Masked Write Command

- DRAM internal hidden read command is generated during write latency.
  - Separated masked write command is required to inform DRAM to generate internal read command.
  - New parity bits are generated after combining unmasked write data with existing cell data.

- Gapless masked write is allowed between different banks only.
  - 4 tCCD (32 clocks) period is required between two masked write operation in same bank.

Masked Write (MWR) Operation

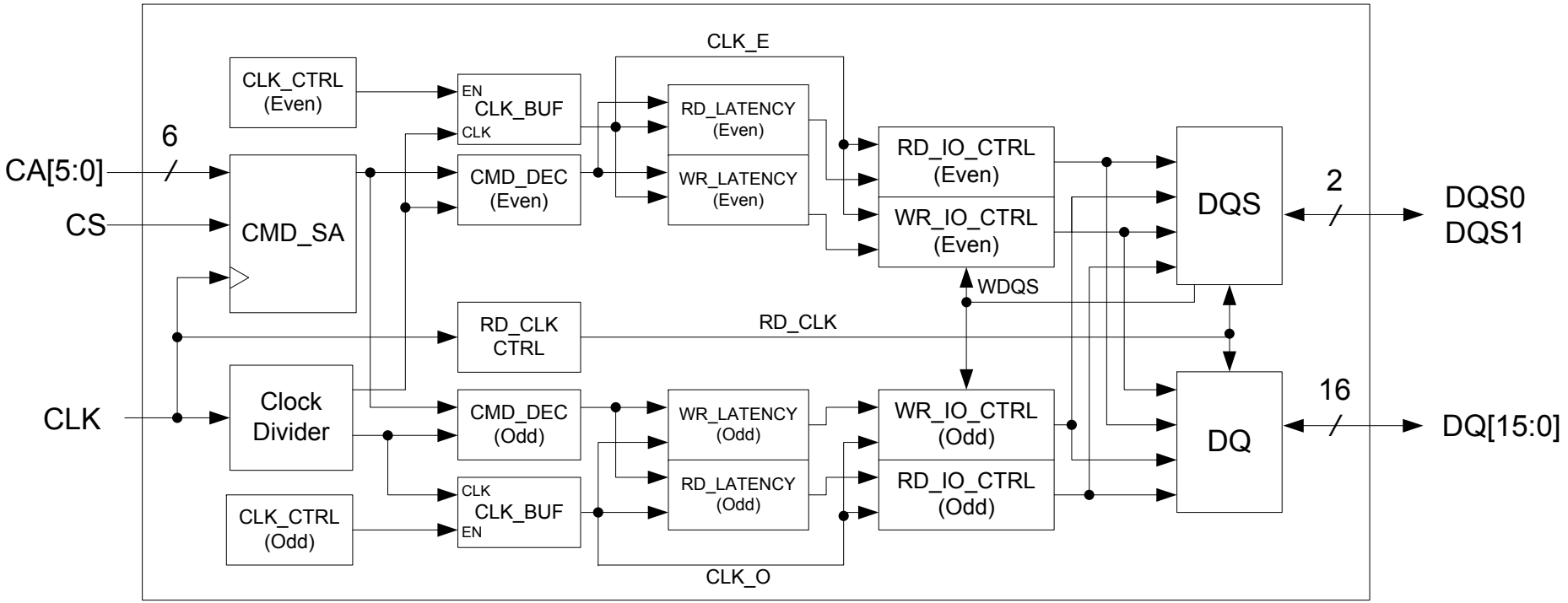


MWR Timing Constraints

	Same Bank				Different Bank			
Next / Current	RD	WR	MWR	Pre charge	RD	WR	MWR	Pre charge
Active	tRCD	tRCD	tRCD	tRAS	tRCD	tRCD	tRCD	tRAS
RD	tCCD	tRTW	tRTW	tRTP	tCCD	tRTW	tRTW	tRTP
WR	tWTR	tCCD	4*tCCD	(WL+1+ BL/2)*tCK +tWR	tWTR	tCCD	tCCD	(WL+1+ BL/2)*tCK +tWR
MWR	WL+1+ BL/2+ tWTR	tCCD	4*tCCD	(WL+1+ BL/2)*tCK +tWR	WL+1+B L/2+ tWTR	tCCD	tCCD	(WL+1+ BL/2)*tCK +tWR

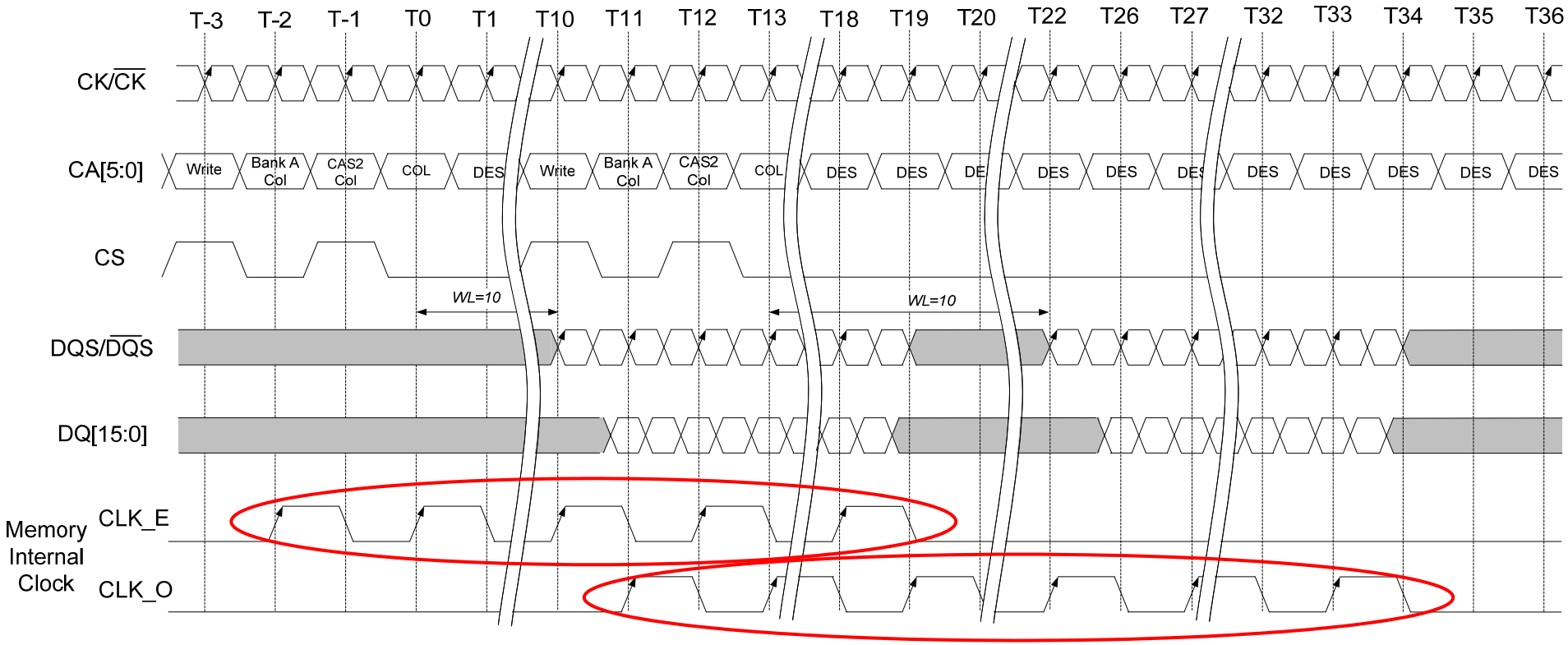
- Gapless WR to MWR, MWR to MWR in same bank is not allowed, due to DRAM internal hidden read operation.

Time Interleaved Latency Control



- At 3.2Gbps, the memory clock is 1.6GHz, and period is only 625ps.
- Each divided clock (CLK_E, CLK_O) has its own command decoder, write & read latency control.
  - Doubled timing margin for DRAM peripheral circuits.

Even/Odd Clock Control



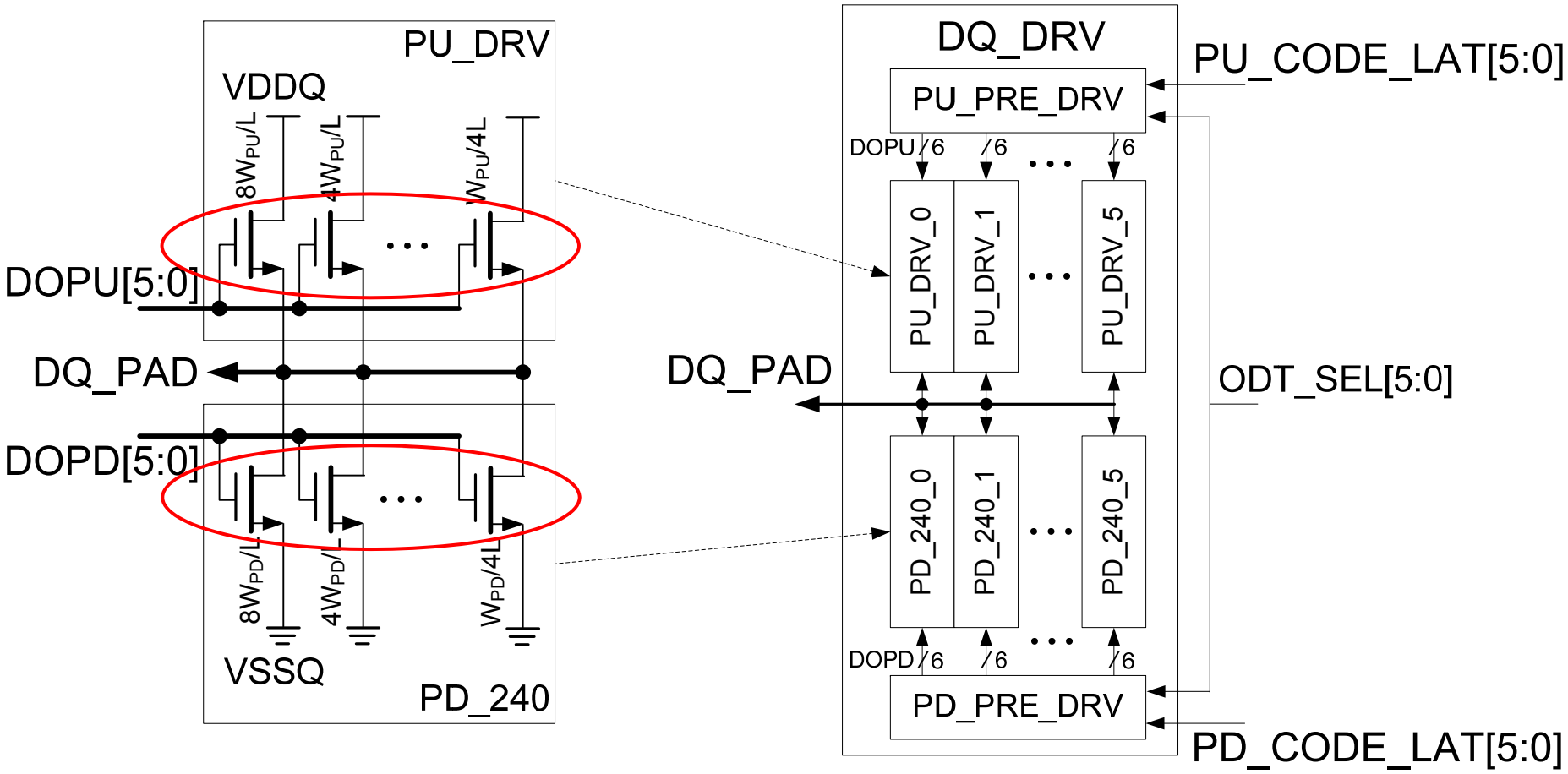
- Each divided clock is enabled when a command at corresponding clock edge is received.

  -> After completing command processing, clock is disabled to reduce current consumption.

LPDDR4 IO

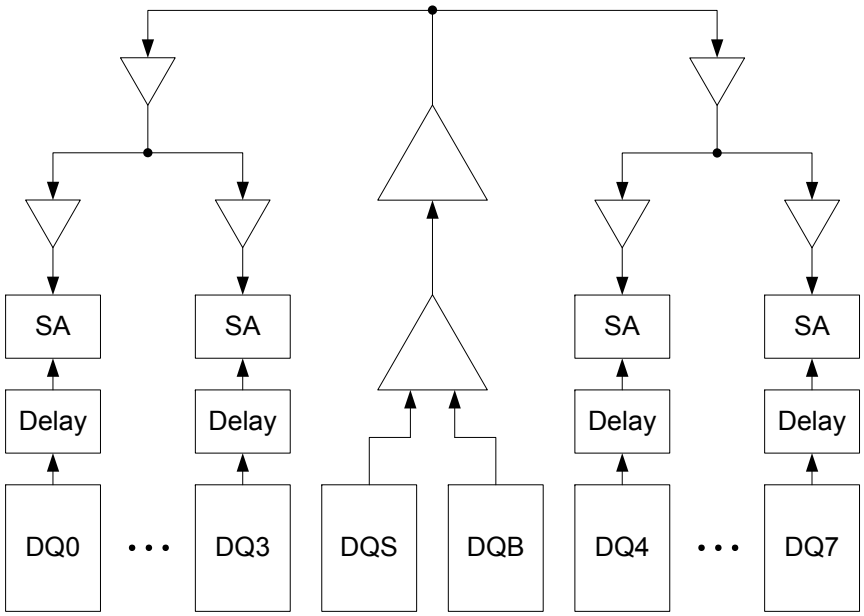
- LVSTL(Low Voltage Swing Terminated Logic) Driver
  - NMOS pull-up & pull-dn drivers
- Unmatched DQ & DQS
  - No extra delay in DQ path
- DQS Oscillator
  - Detect delay variation in DQS tree
- FIFO based Write & Read Training
- ZQ Calibration
  - VOH (VDDQ/3 or VDDQ/2.5) calibration
  - Separated ZQ CAL Start & Latch commands

LVSTL IO



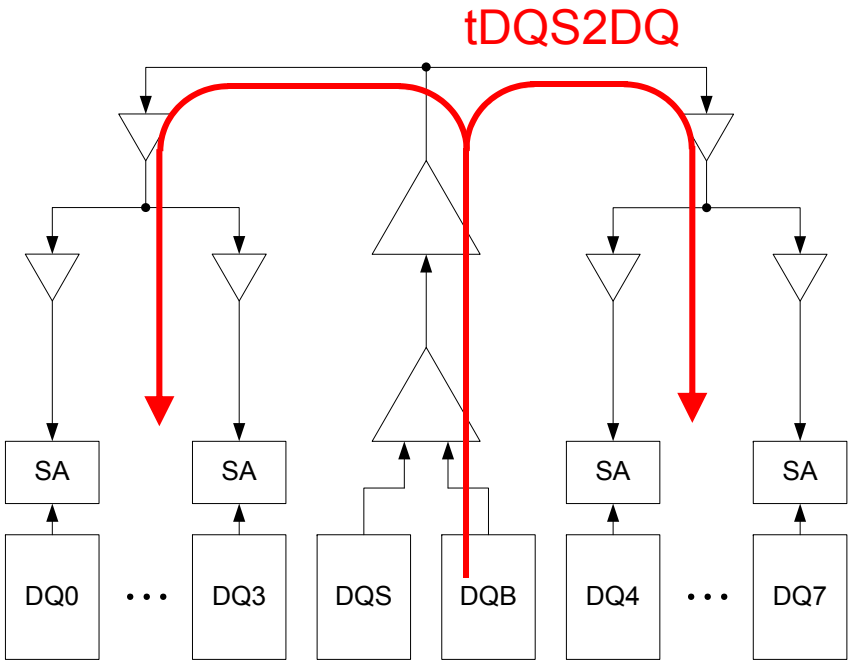
- NMOS pull-up & pull-dn drivers.
  - VOH level is digitally calibrated by DOPU[5:0].

Unmatched DQ & DQS



Conventional

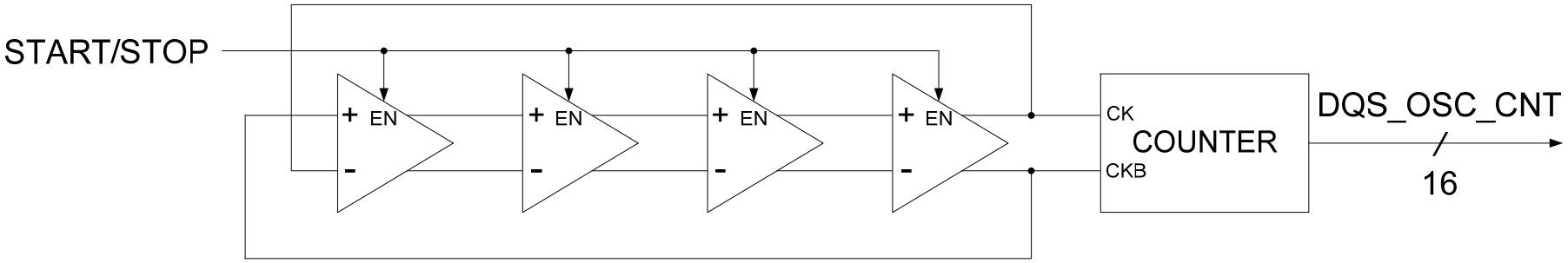
- Extra delay in DQ path matches DQS path delay.
- Require high BW delay path in each DQ.



LPDDR4

- SA directly samples received data. (Current reduction & superior SI)
- DRAM controller is responsible for DQS path delay (tDQS2DQ) compensation.

DQS Oscillator



Ring oscillator of DQS tree replica.

- Indirect measurement of tDQS2DQ through replica delay.

  - DQS_OSC_CNT increases by 1 whenever “2 X tDQS2DQ” passes.

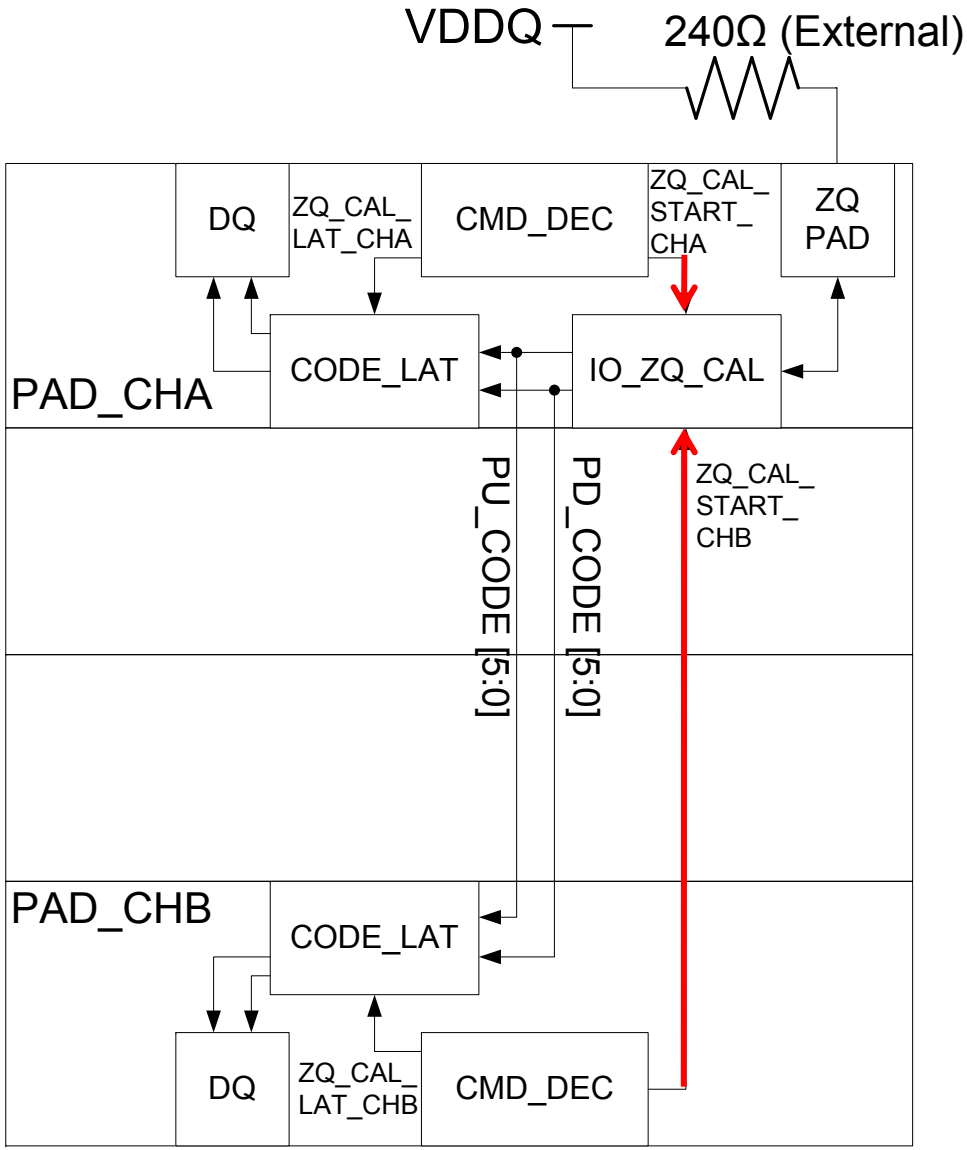
  Ex) DQS oscillator enable period = 100ns.
  DQS_OSC_CNT value = 100.

  tDQS2DQ = 100ns ÷ 100 ÷ 2 = 500ps

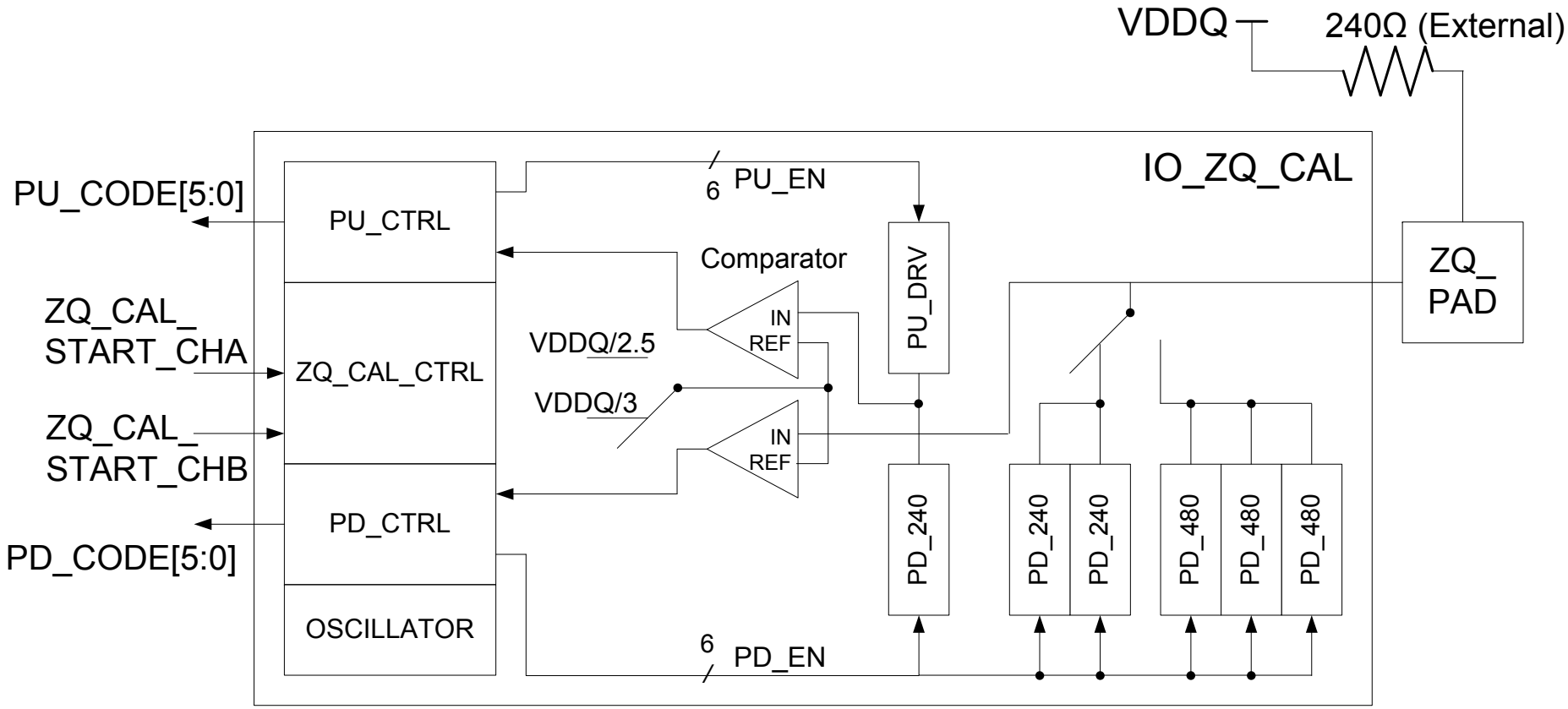
- Controller can adjust DQS timing or retrain IO.
  after reading DQS_OSC_CNT value.

ZQ Calibration Circuit

- ZQ calibration circuit and external resistor are shared between two channels.
- ZQ calibration sequence can be initiated from both channels.



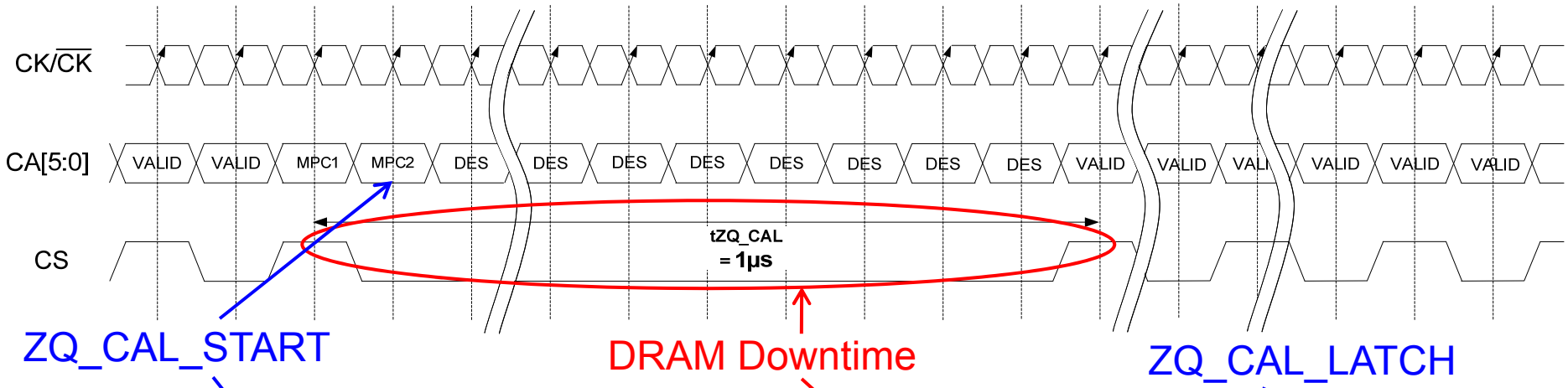
IO_ZQ_CAL



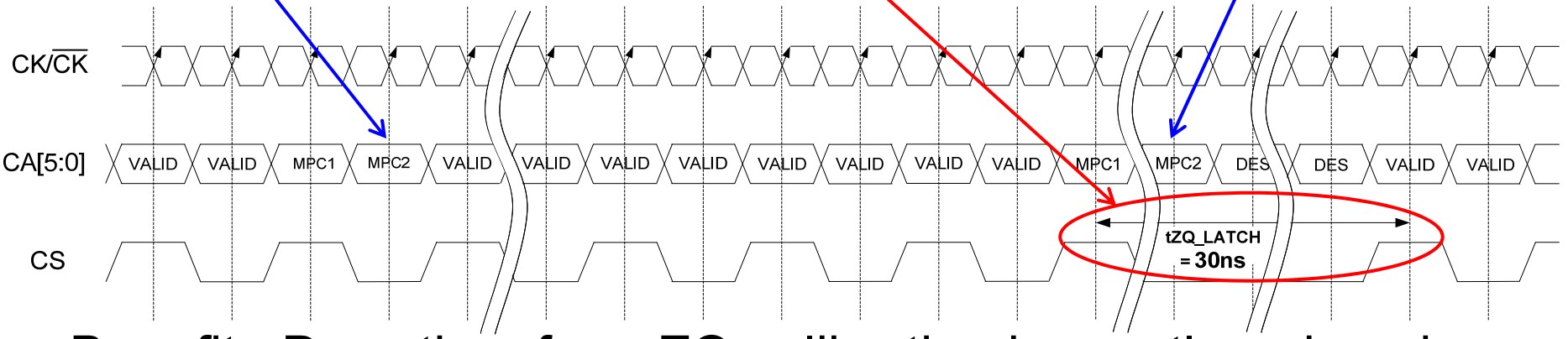
- PD drivers are calibrated to 120ohm or 160ohm depending on VOH level configuration.
- PU drivers are calibrated to match VDDQ/3 or VDDQ/2.5 output level.

ZQ_CAL_START/LATCH

Conventional Devices : No CMD allowed during ZQ CAL

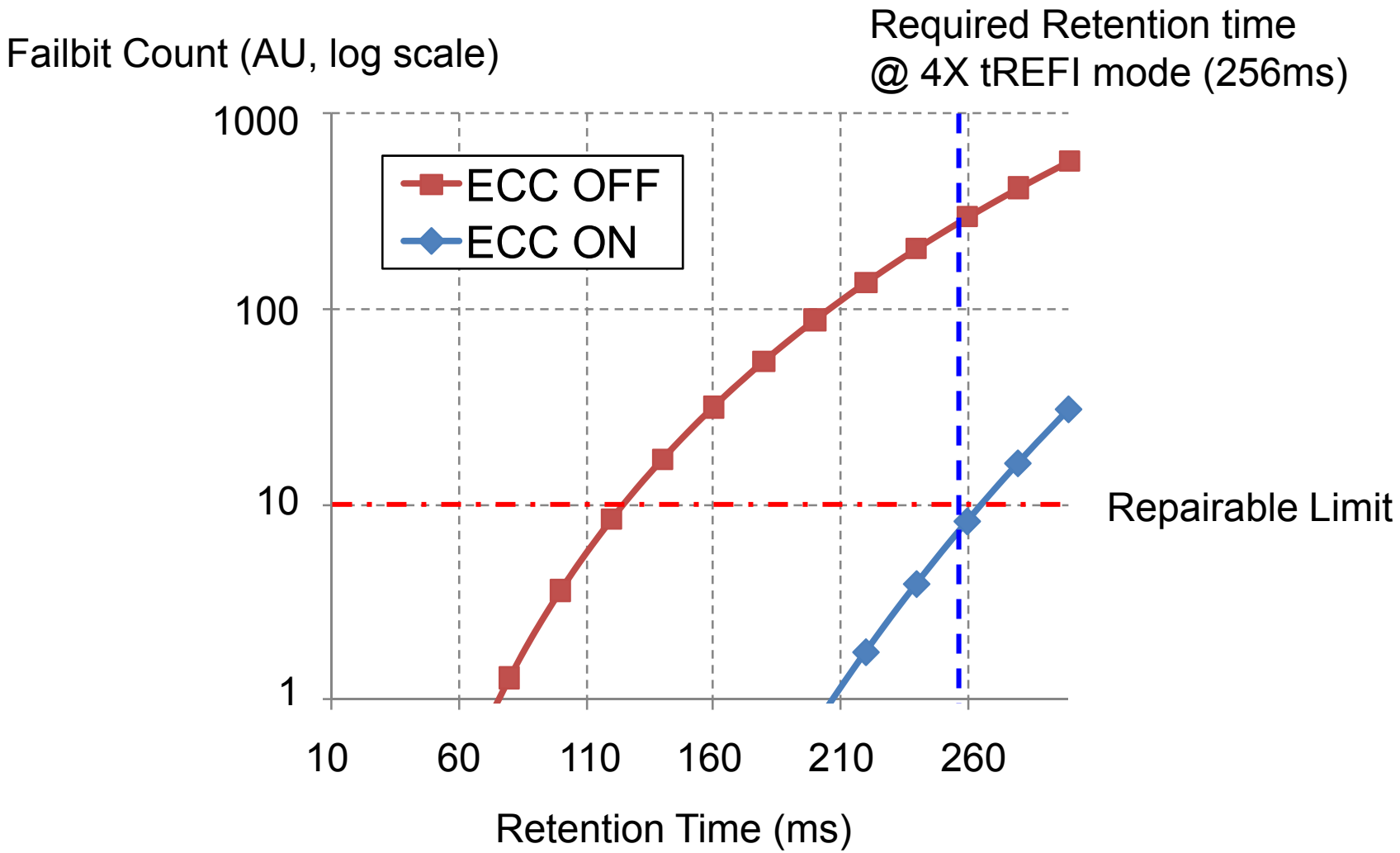


LPDDR4 : No CMD allowed only when updating ZQ CAL result to IO



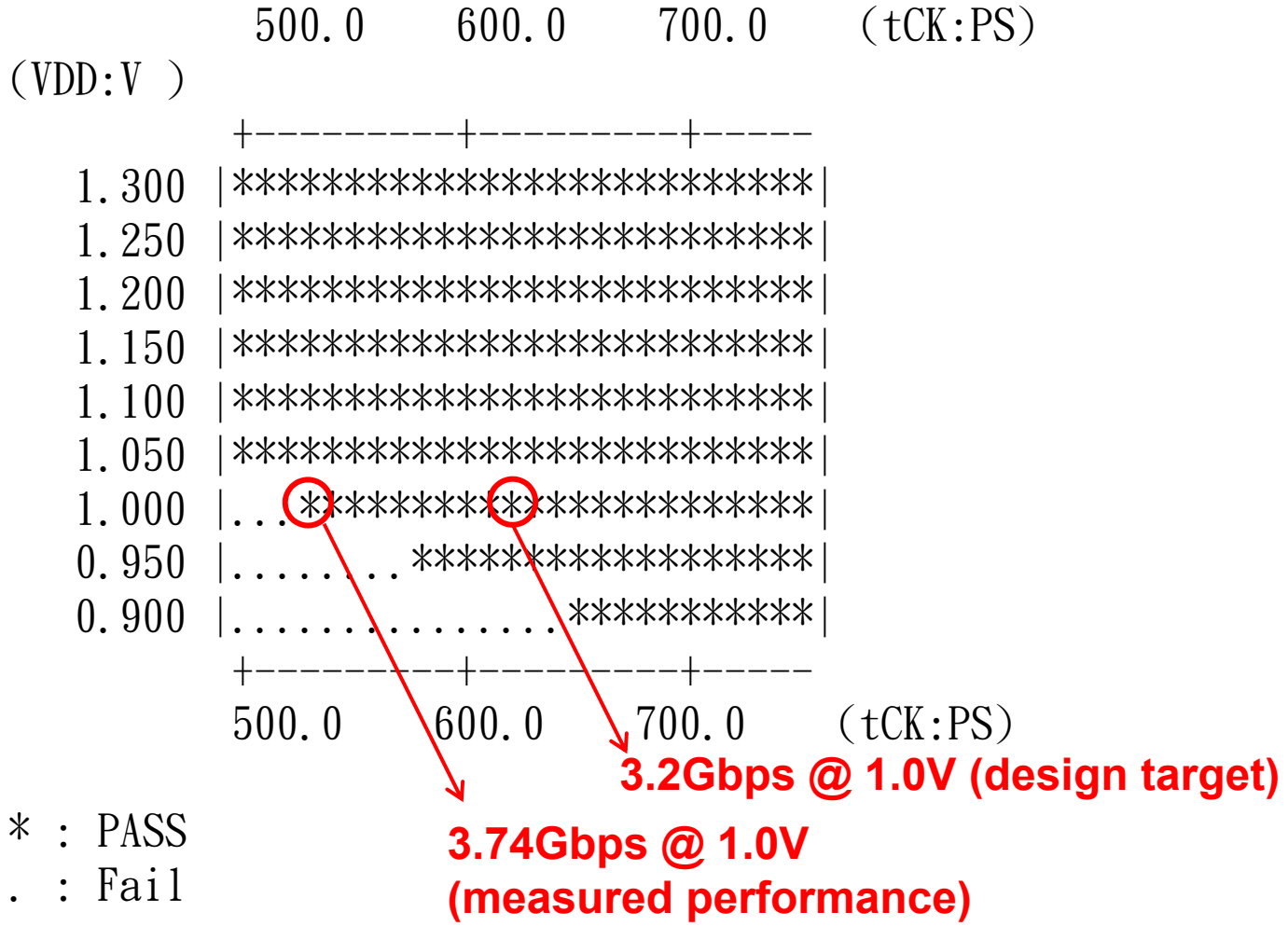
Benefit : Downtime from ZQ calibration is greatly reduced.
Frequent periodic ZQ calibration is possible.

Failbit Measurement Result



Measurement Condition : 25°C, 0.85V supply voltage.

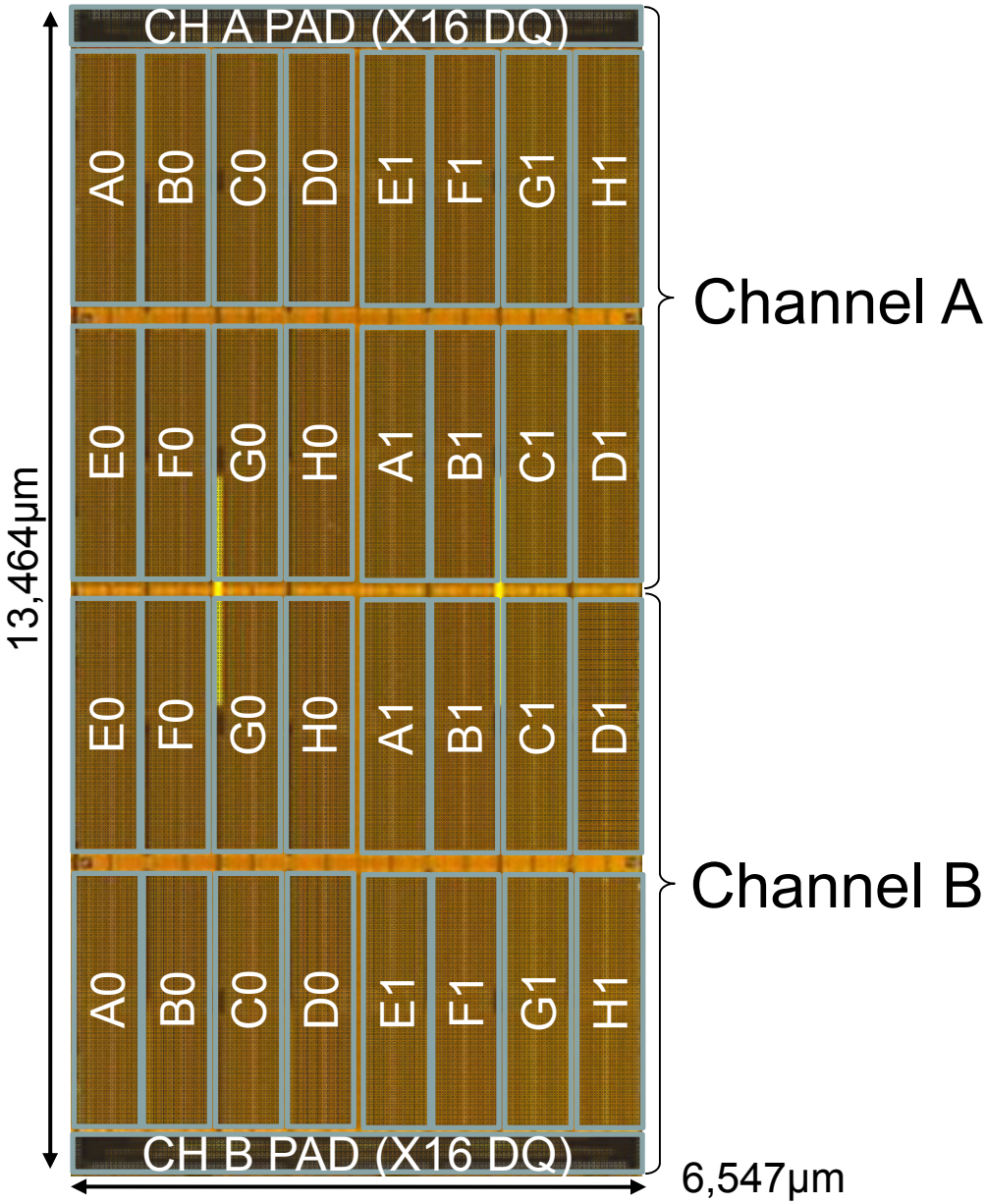
tCK Shmoo



Chip Summary

Process	25nm CMOS 3 metal
Package	272 ball POP
Data Rate	3.2Gbps/pin (@RL32, RDBI=on)
No. of Channel	2 Channel per Die
Banks	8 banks per channel
Capacity	128Mx32b per channel
Burst Length	16 Burst Length (MRS BL32 support)
Number of IO's	x16 I/O per channel
Die Area	Area : 88.1mm^2
Supply Voltage	1.0V

Die Photograph



Conclusion

- The first commodity DRAM
  with integrated ECC engine.
  - New MWR command for DM operation
  - DRAM internal read-modify-write with ECC correction.

- 3200Mbps per pin operation
  - Time interleaved latency control
  - Even/Odd clock control for current reduction
  - Unmatched DQ and DQS with pin-to-pin IO training
  - Periodic training including ZQ calibration

A 1.2V 8Gb 8-Channel 128GB/s High-Bandwidth Memory (HBM) Stacked DRAM with Effective Microbump I/O Test Methods Using 29nm Process and TSV

Dong Uk Lee, Kyung Whan Kim, Kwan Weon Kim, Hongjung Kim,
Ju Young Kim, Young Jun Park, Jae Hwan Kim, Dae Suk Kim,
Heat Bit Park, Jin Wook Shin, Jang Hwan Cho, Ki Hun Kwon, Min Jeong Kim,
Jaejin Lee, Kun Woo Park, Byongtae Chung, Sungjoo Hong

SK Hynix

Outline

- **Introduction**
- **8Gb High Bandwidth Memory(HBM) Features**
  - 5-Hi Stacked DRAM architecture
  - Dual row/column command interface
  - Clocking, parity and loopback
  - Microbump impedance monitoring
  - Test method
- **Measurements and Chip Micrograph**
- **Summary**

Introduction

- **Increasing demands of higher bandwidth**
  - High performance computing(HPC) memory, network memory(TbE), graphics memory
  - Over 500GB/s bandwidth
- **How to achieve?**
  - **Narrow width I/O and higher speed (25~50GB/s)**
    - Need additional circuitry : On-die-term., PLL, ISI & crosstalk reduction
    - More than a dozen memory chips are needed
  - **Wide width I/O and lower speed (128GB/s~)**
    - Native signaling, minimum additional circuitry
    - Only 4 memory chips are needed

Limitations of Wide I/O Memory

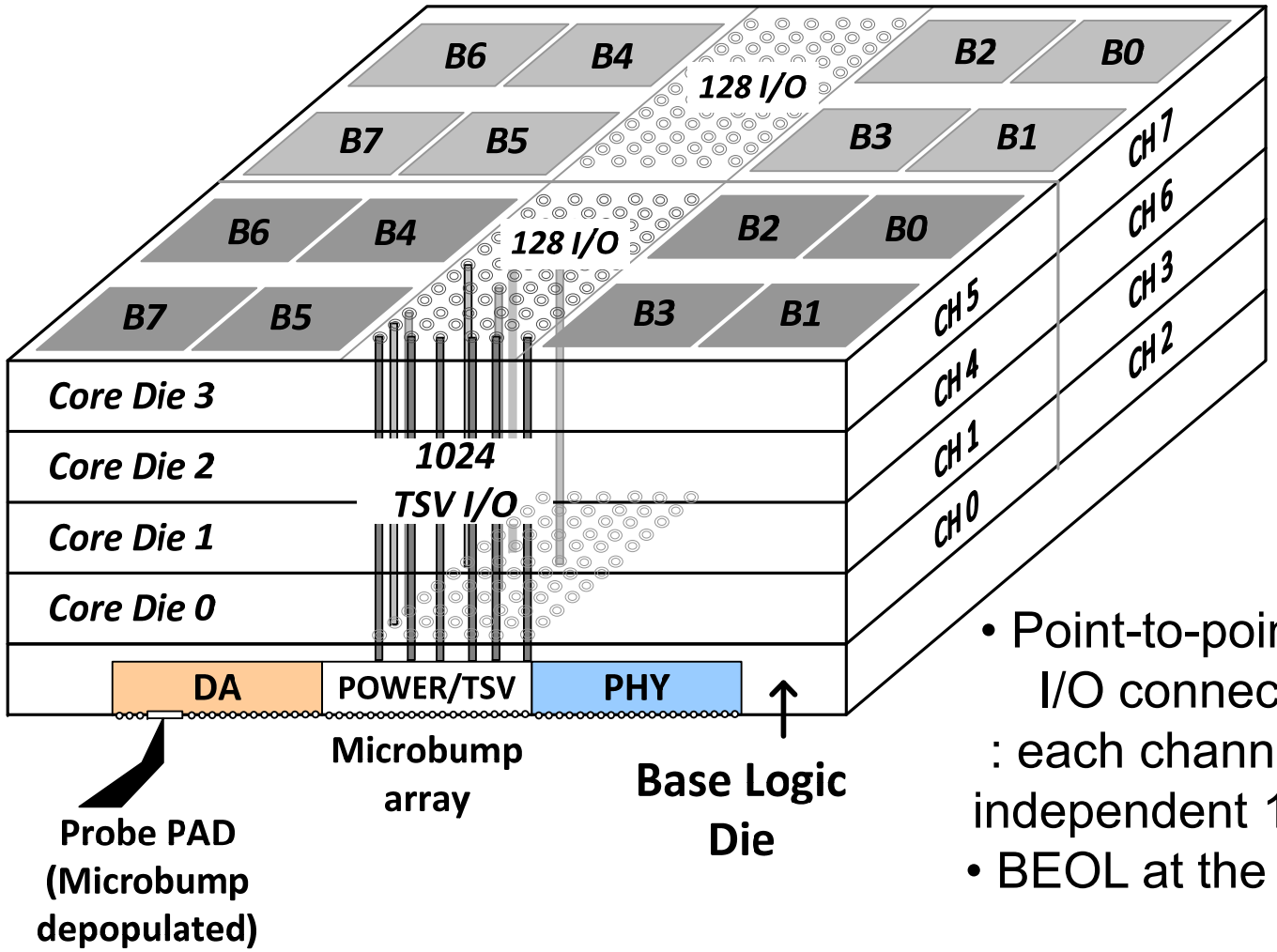
- **How to test the microbump interface?**
- **How to guarantee the cell and TSV?**
- **How to manage power distribution?**

→ Solution : Base logic die

- **Various test method** (including DA & serial port)
- **MBIST**(Memory-Built-In-Self-Test) & cell repair
- **Redistribution of power** plane and reduced C_{IO} by short distance between PHYs

HBM Stacked-DRAM Architecture

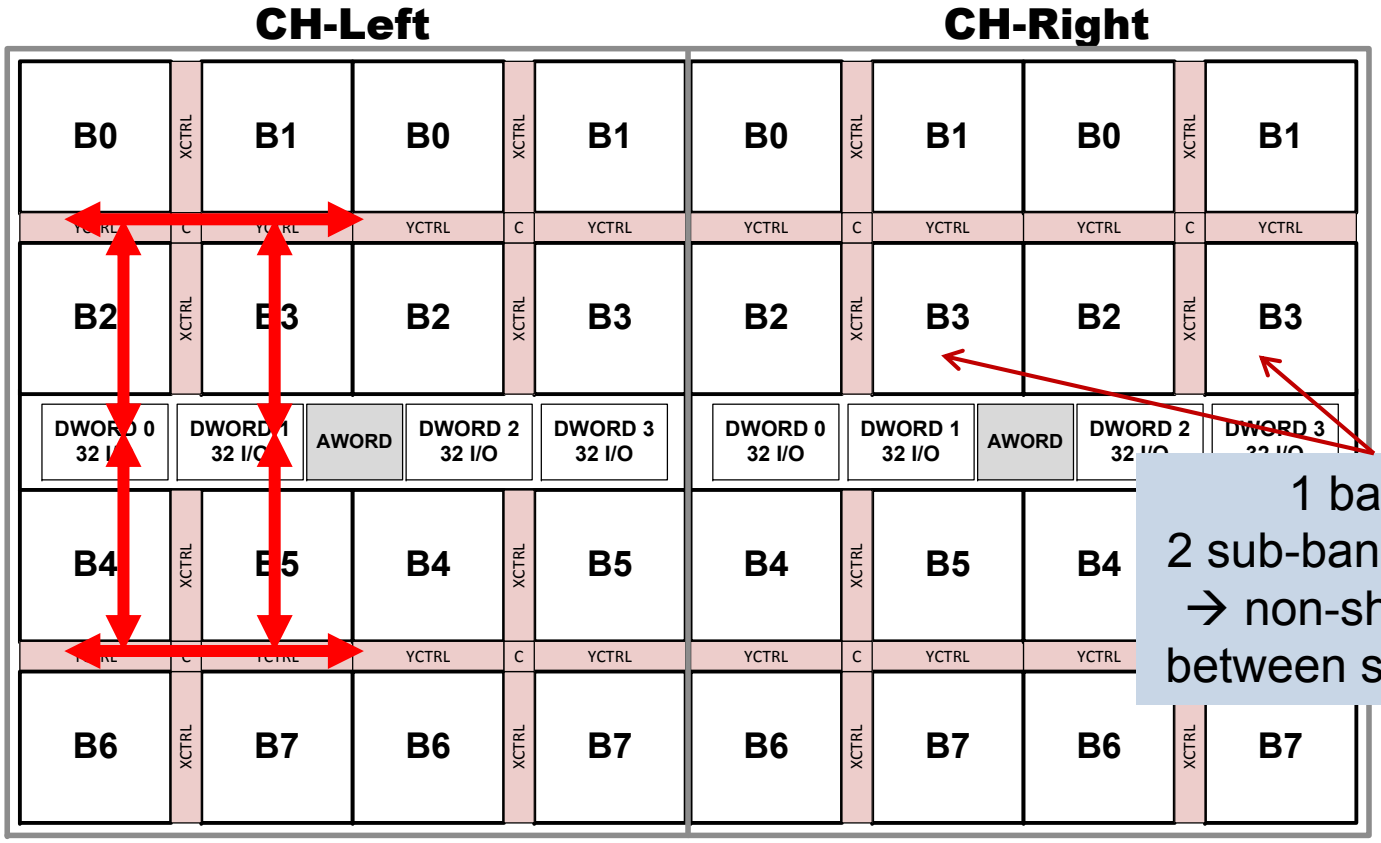
- 4 DRAM + 1 Base Logic Die (Chip-on-Wafer)



- Point-to-point TSV I/O connection : each channel has independent 128 I/O
- BEOL at the bottom

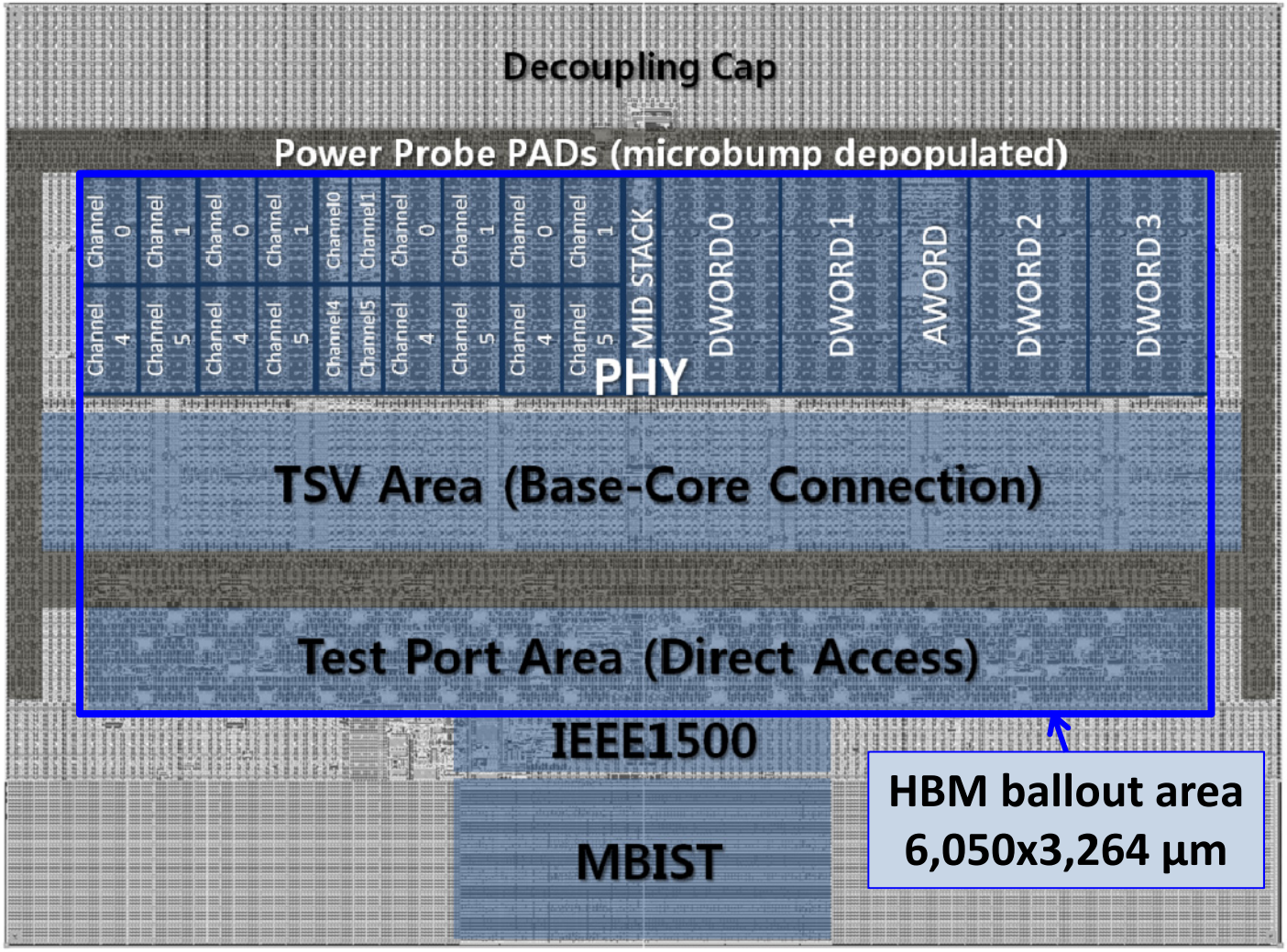
Core Architecture

- **1 slice has 2 channels, a channel consists of**
  - 8 bank(16-sub bank), 128 TSV I/O, 2*n*-prefetch
  - 256 global I/O → 32B access granularity



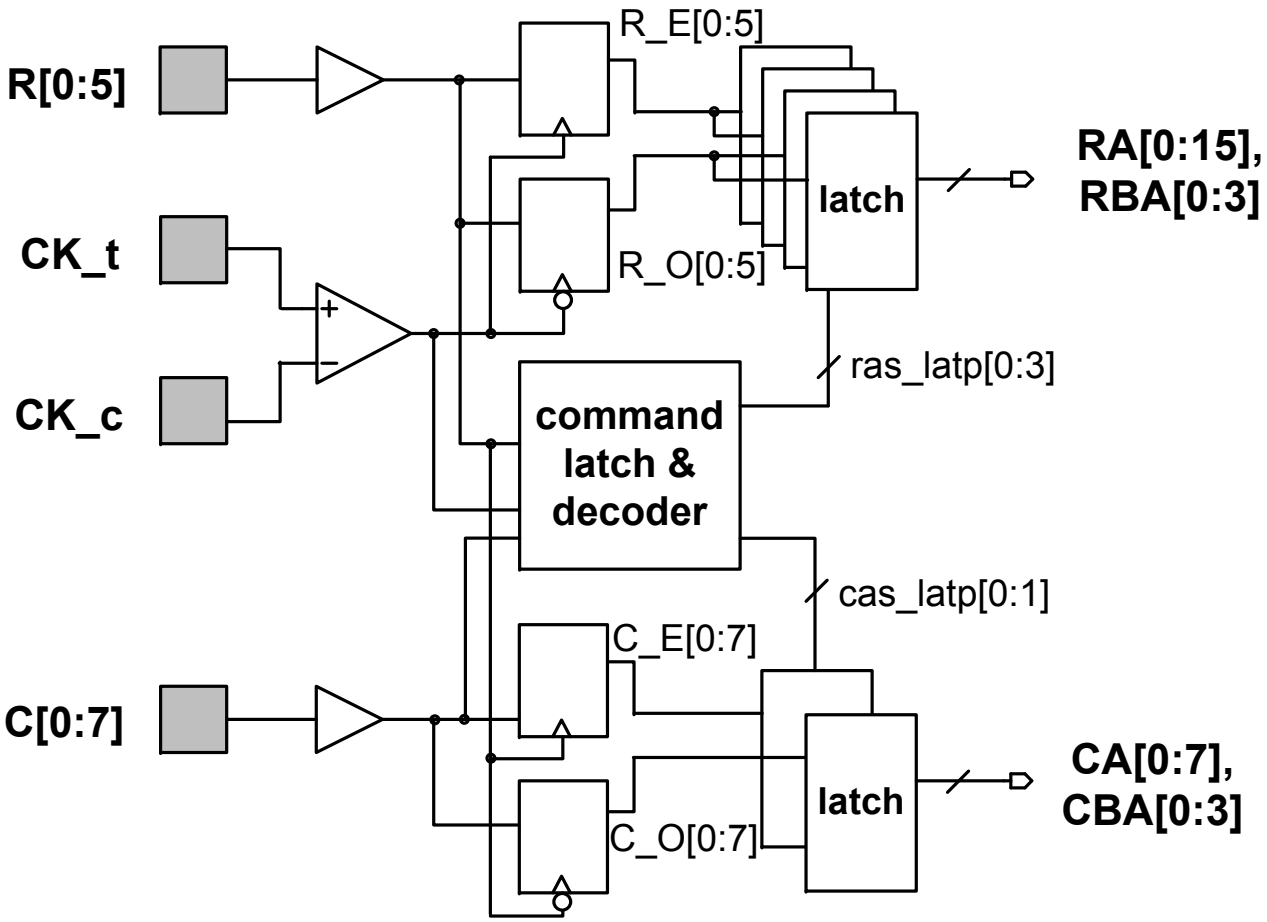
Functionality of Base Logic Die

- PHY has 1024 I/O interface (128 I/O x 8 ch)



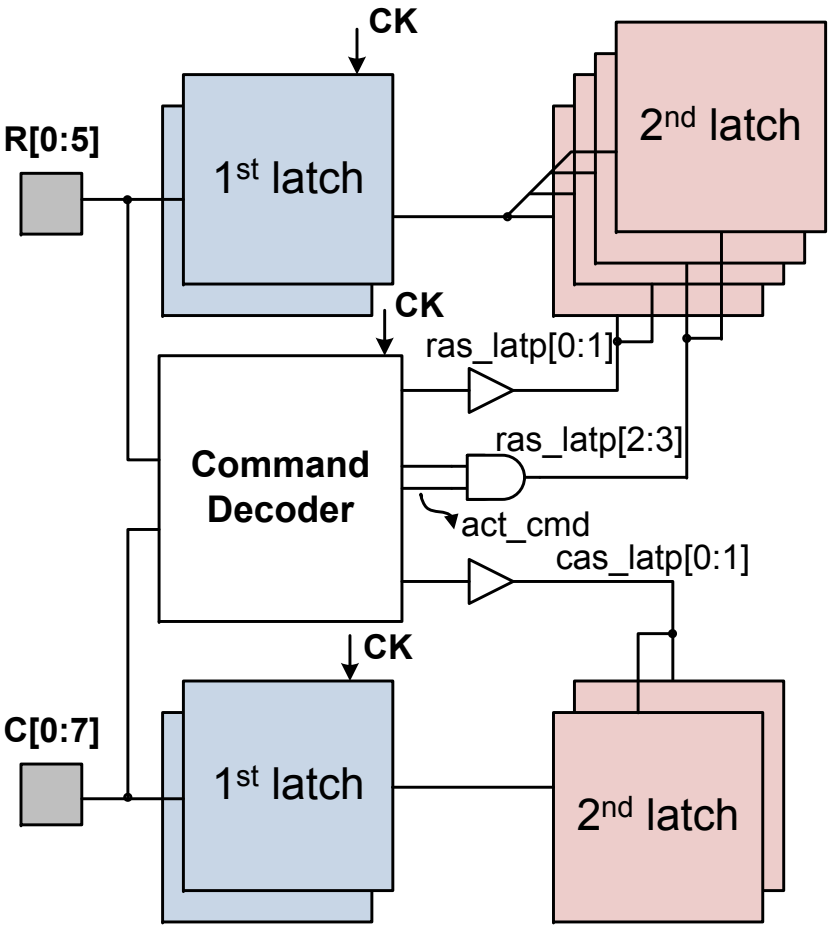
Dual Command Interface

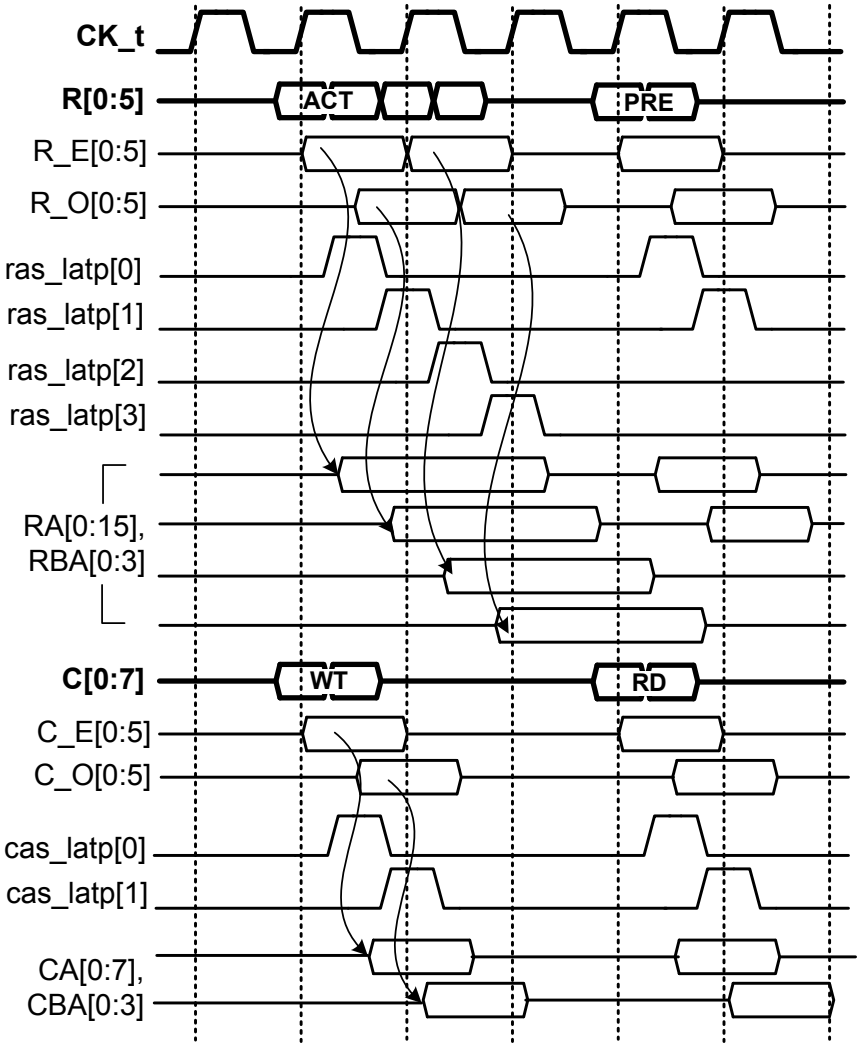
- **Semi-independent row/column input**
  - Row/column input through different pin



Dual Command Interface

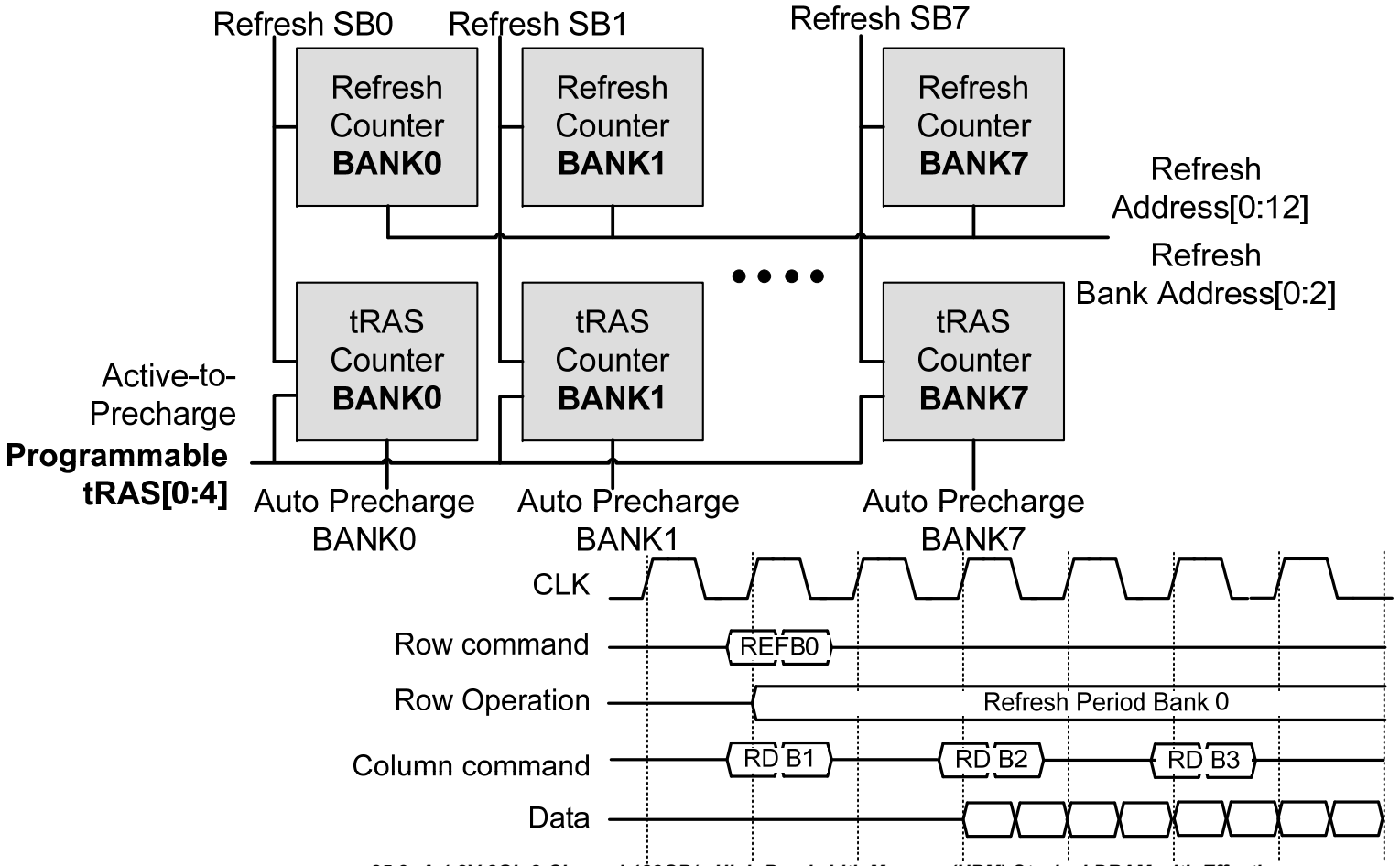
- **Timing diagram**





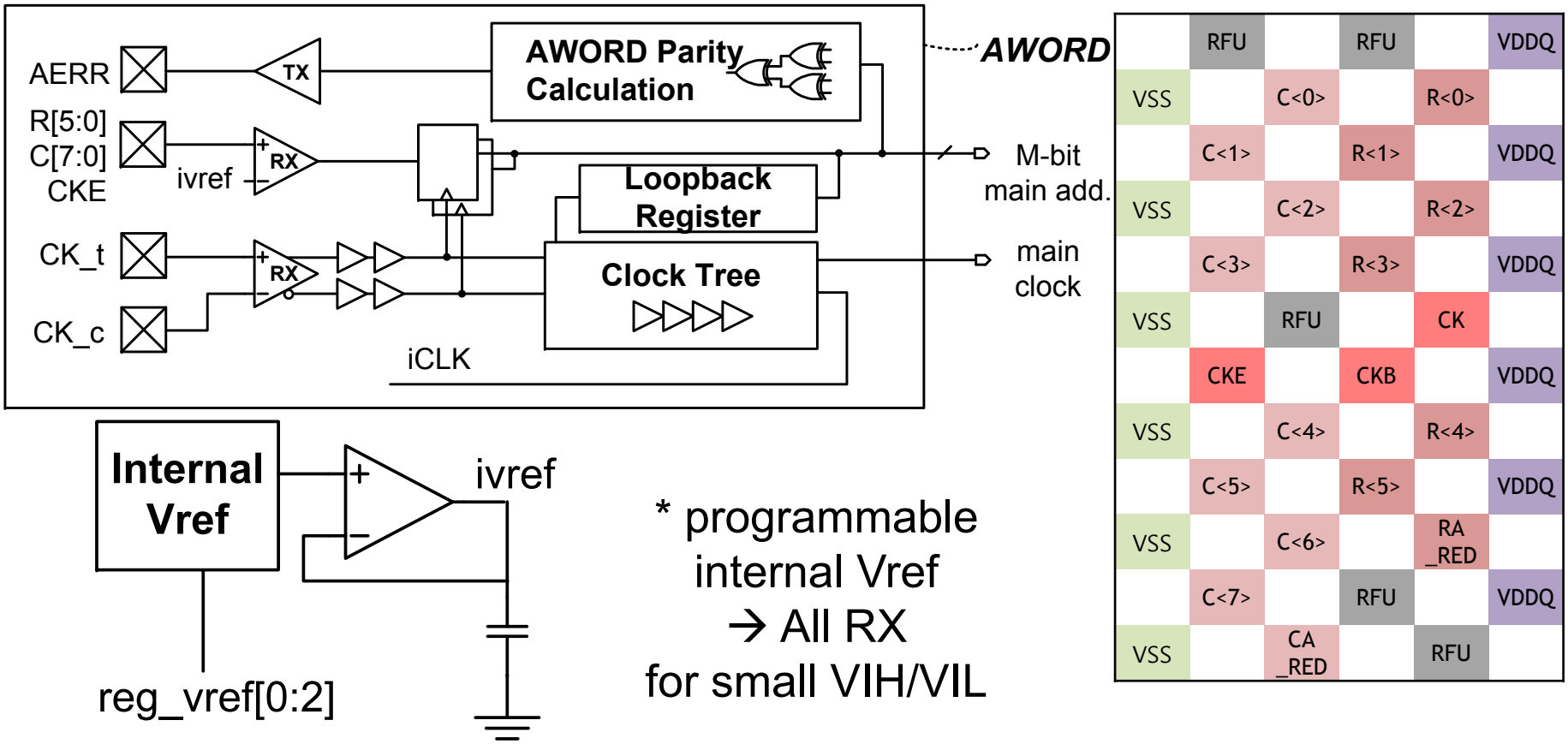
Special Operation Functions

- **Single bank refresh and programmable tRAS**
  - Refresh cycle can be completely hidden



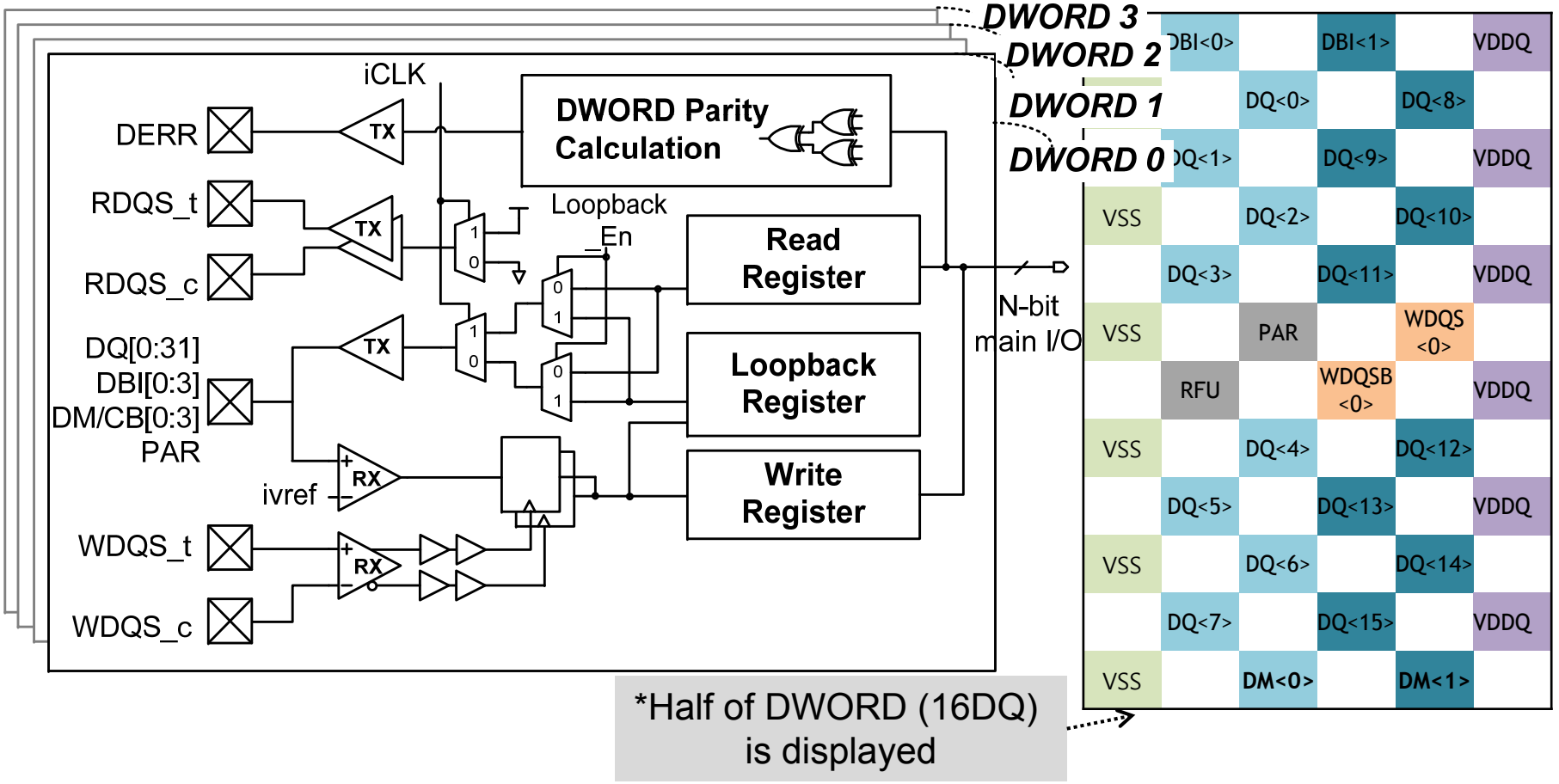
Clocking Scheme of HBM (AWORD)

- **Differential clock & DDR addressing**
  - AWORD(address buffer) with parity and loopback



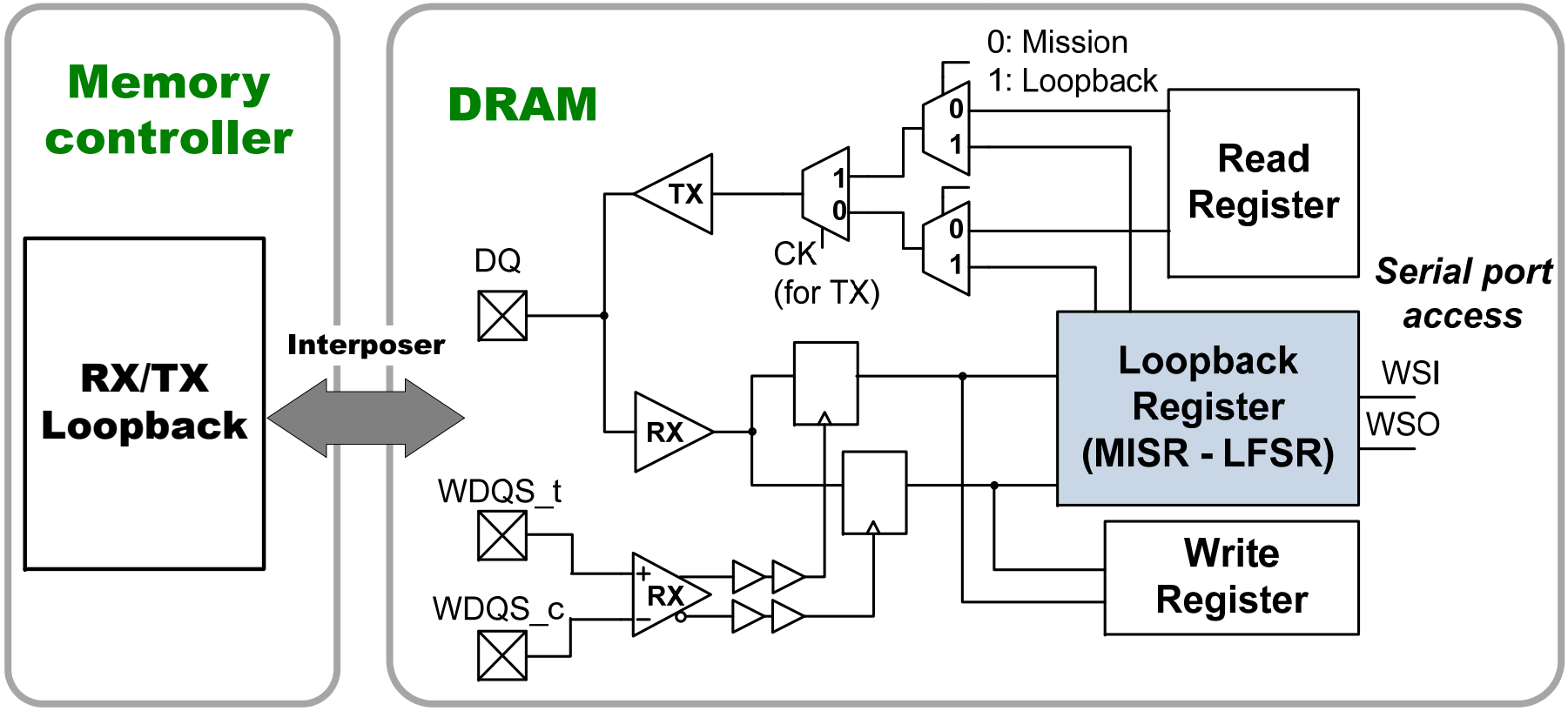
Clocking Scheme of HBM (DWORD)

- **Unidirectional differential W/R strobes / 32DQ**
  - 4 DWORD(data buffer)/channel (with parity & loopback)



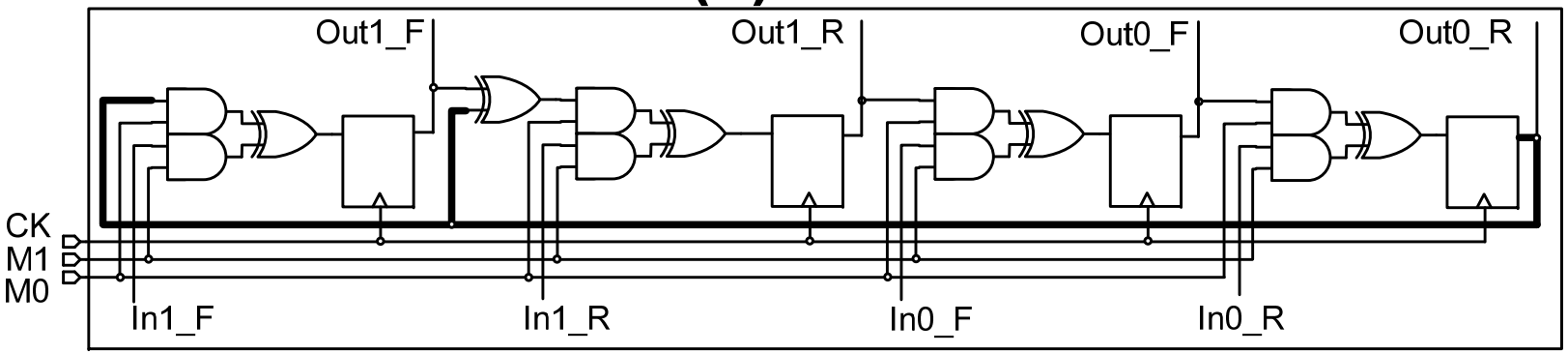
Loopback Function

- **Loopback(MISR-LFSR) design for I/O link testing and training**
  - Between memory and controller (Wt: MISR, Rd:LFSR)



MISR/LFSR Calculation

- **4bit MISR/LFSR : $f(x)=x^4+x^3+1$**



- **DWORD polynomial : $f(x)=x^{20}+x^{17}+1$**
  - DQ[0:7], DBI, DM (10 I/O pins with DDR)

DWORD 20BIT LFSR Sequence

# of Cal	LSB DM	DM F	DQ[0]	DQ[0] F	DQ[1]	DQ[1] F	DQ[2]	DQ[2] F	DQ[3]	DQ[3] F	DQ[4]	DQ[4] F	DQ[5]	DQ[5] F	DQ[6]	DQ[6] F	DQ[7]	DQ[7] F	DBI	MSB DBI F
Initial	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	1	1	1
3	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	1	1	1
4	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	1
5	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1	1
6	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1
7	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	1	1	1
8	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1
9	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1
10	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1
11	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1
12	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
13	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
14	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
15	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
16	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
18	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0

LFSR calculation results :initial all 1

M [1:0]	MISR Control
00	Sync Reset
01	LFSR
10	Register
11	MISR

MISR/LFSR Calculation

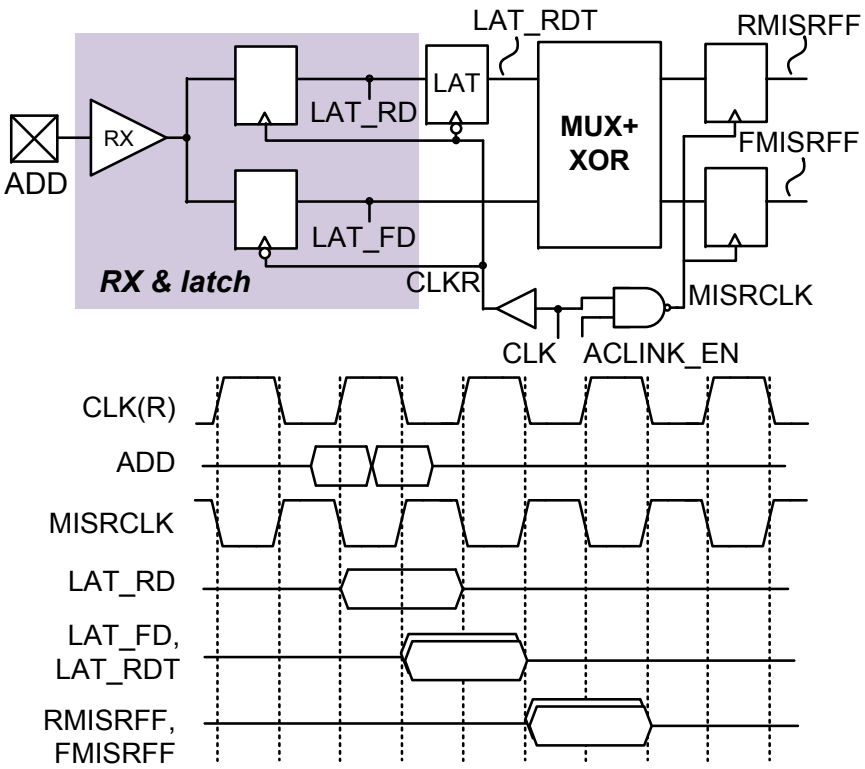
- **AWORD polynomial : $f(x)=x^{30}+x^{6}+x^{4}+x+1$**
  - 15 Address pins(R[0:5], C[0:7], CKE) with DDR
  - MISR_MASK function is supported for neglecting certain pin's test result

AWORD 30BIT LFSR Sequence

LSB … MSB

# of Cal	C[0]	C[0]F	C[1]	C[1]F	C[2]	C[2]F	C[3]	C[3]F	CKE	CKEF	C[4]	C[4]F	C[5]	C[5]F	C[6]	C[6]F	C[7]	C[7]F	R[0]	R[0]F	R[1]	R[1]F	R[2]	R[2]F	R[3]	R[3]F	R[4]	R[4]F	R[5]	R[5]F
Initial	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
3	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
4	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0
5	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0
6	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1
7	1	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0
8	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1
9	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1
10	0	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1
11	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1	0
12	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1
13	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1
14	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1
15	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1
16	1	0	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1
17	1	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1
18	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1
19	1	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1
20	1	1	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	0	1	0	1	1	1	0	1

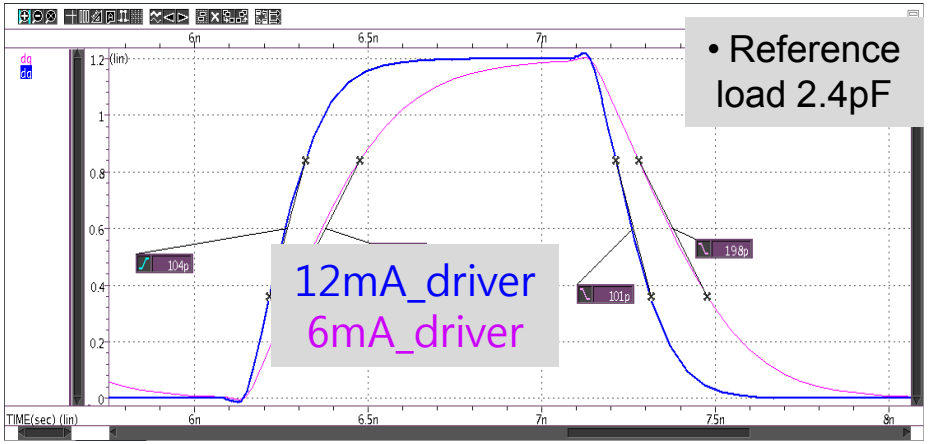
LFSR calculation results :initial all 1

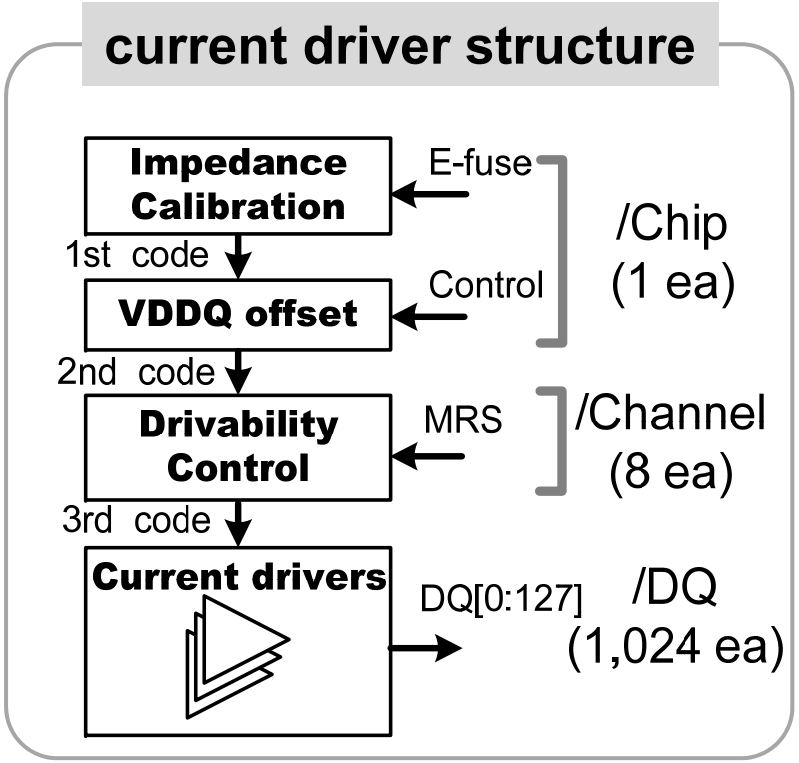


Current Driving

- **HBM drivers have programmable current setting (load model → lumped capacitance)**
  - CMOS driver(with calibration) simulation results has close similarity with ideal current driver(VDDQ:1.2v)

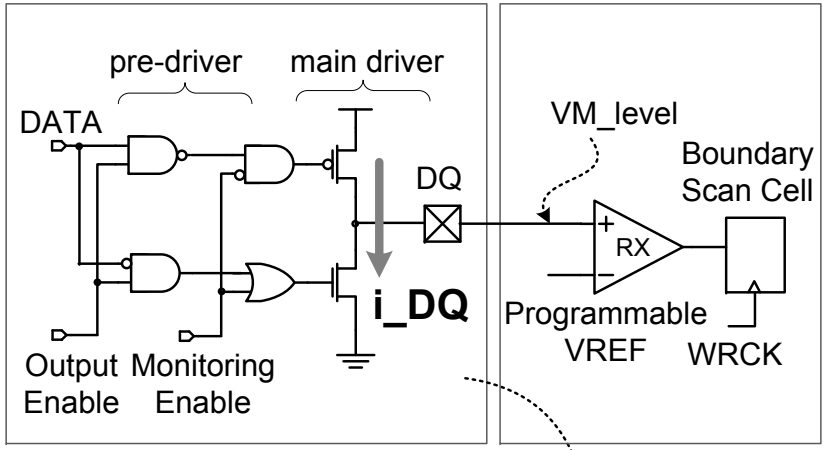
Driver	Rising time	Falling time
6mA (0.6v / 100Ω)	197ps	198ps
12mA (0.6v / 50 Ω)	104ps	101ps
Ideal 12mA driver	100ps	100ps

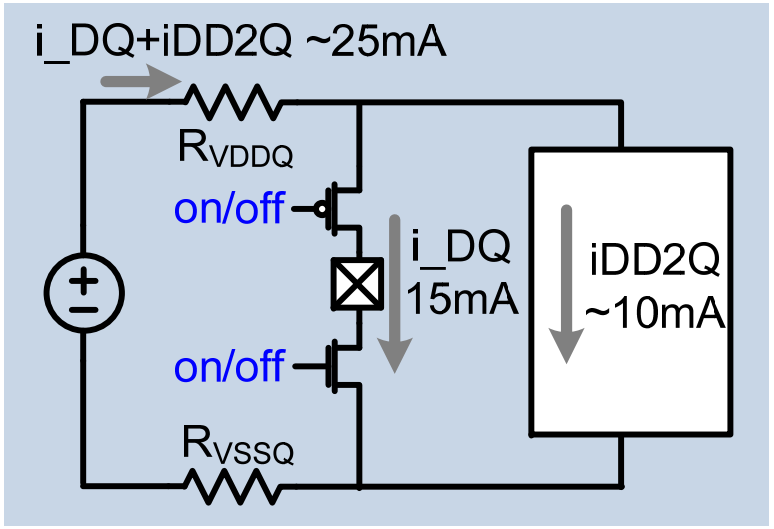


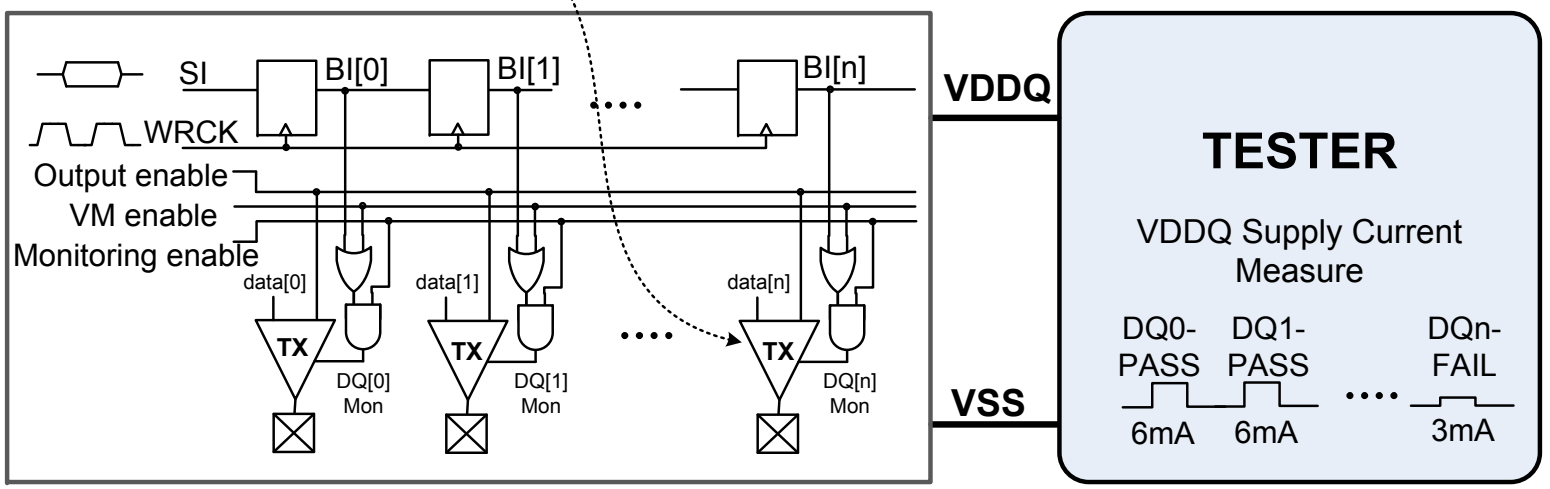


Microbump Impedance Monitoring

- **i_DQ current measure**
  - Without touching PAD

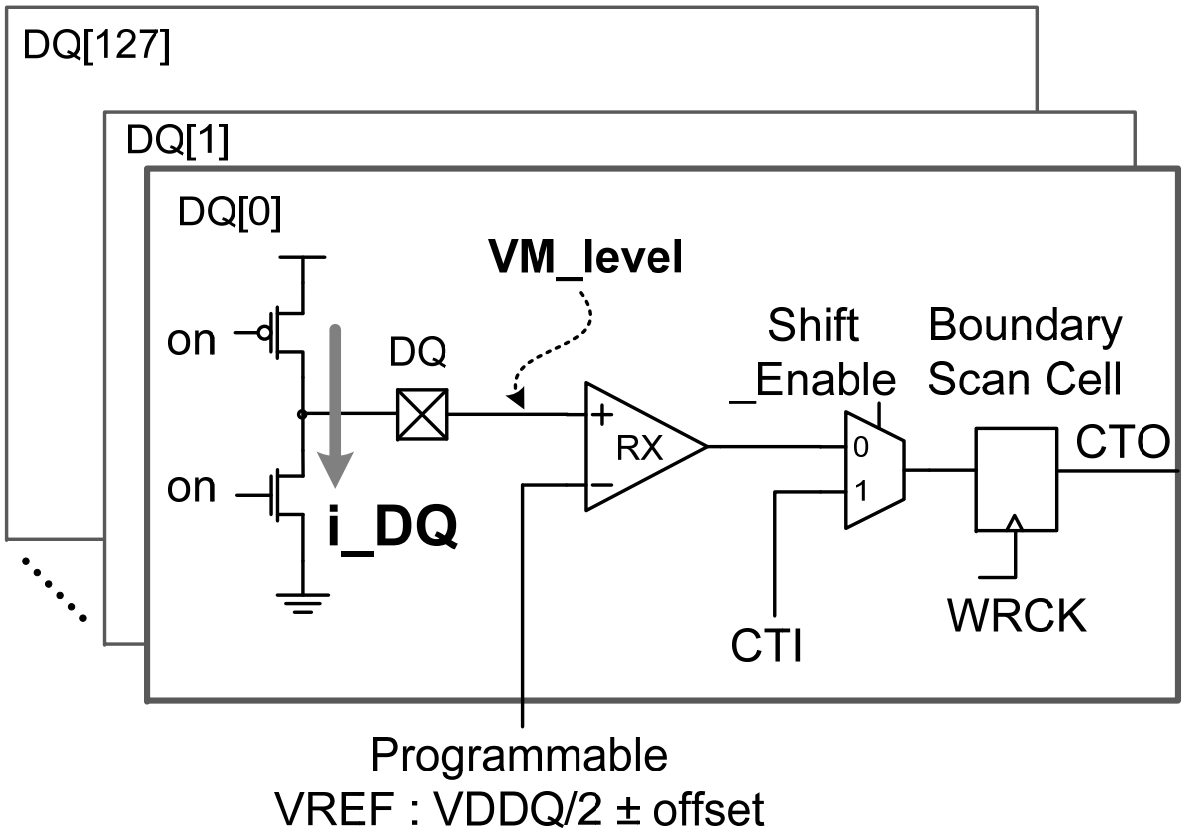






Microbump Impedance Monitoring

- **VM_level measuring**
  - Method of detecting pullup/pulldown impedance mismatch



VDDQ/2 + offset → Vref

Measure (RX → register)

Shift out (128DQ : all 0)

VDDQ/2 - offset → Vref

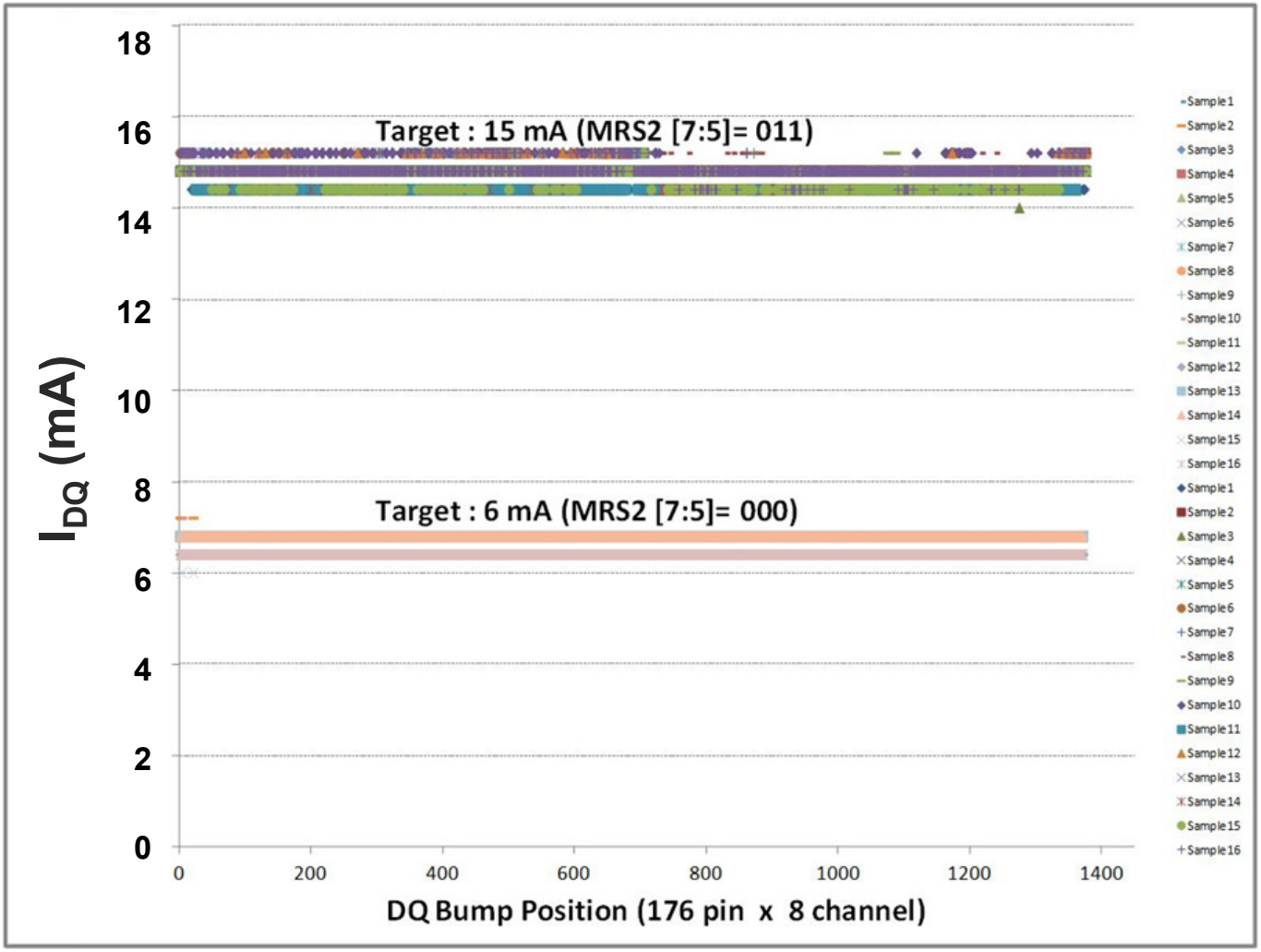
Measure (RX → register)

Shift out (128DQ : all 1)

VM(128DQ) :
within VDDQ/2 ±offset

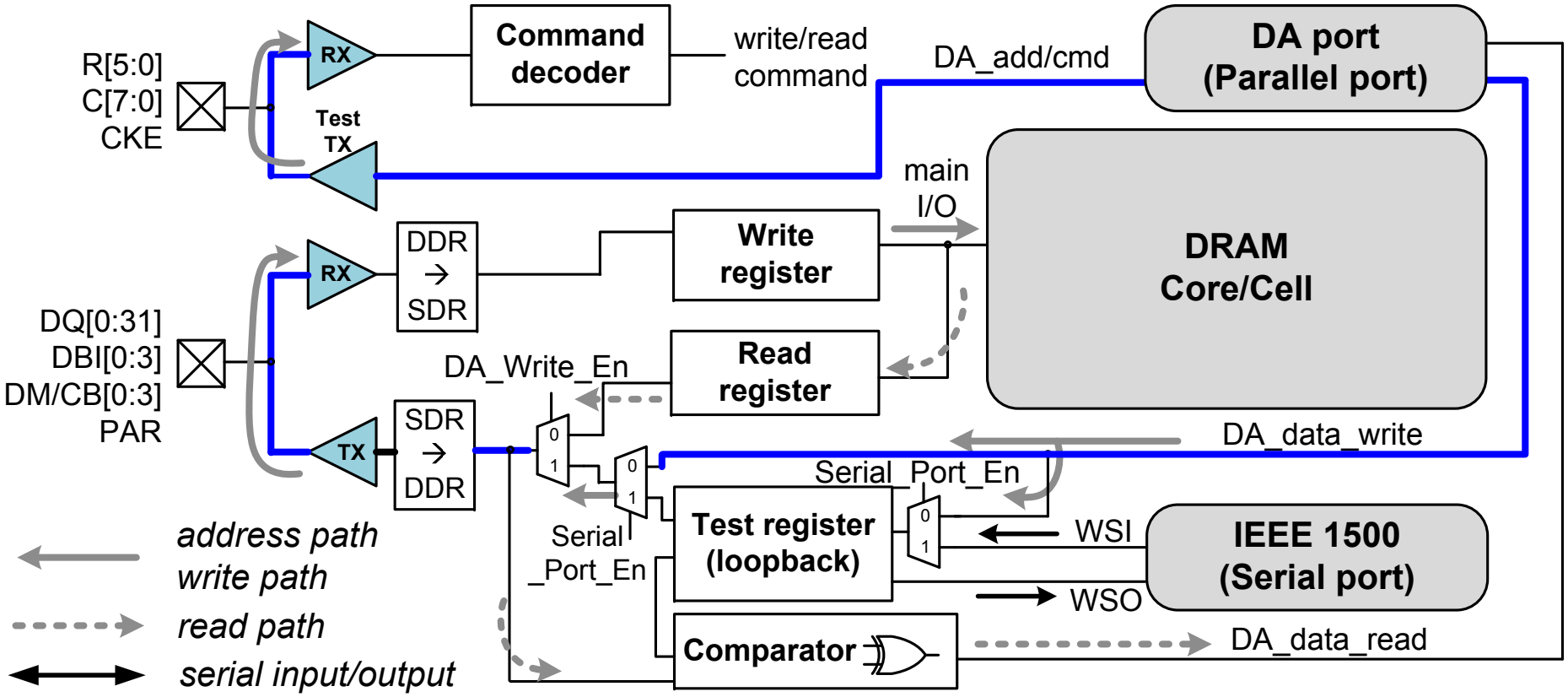
TX Impedance Measurement w/o Probing

- 1408 IO of 16 chips have target current ±10%



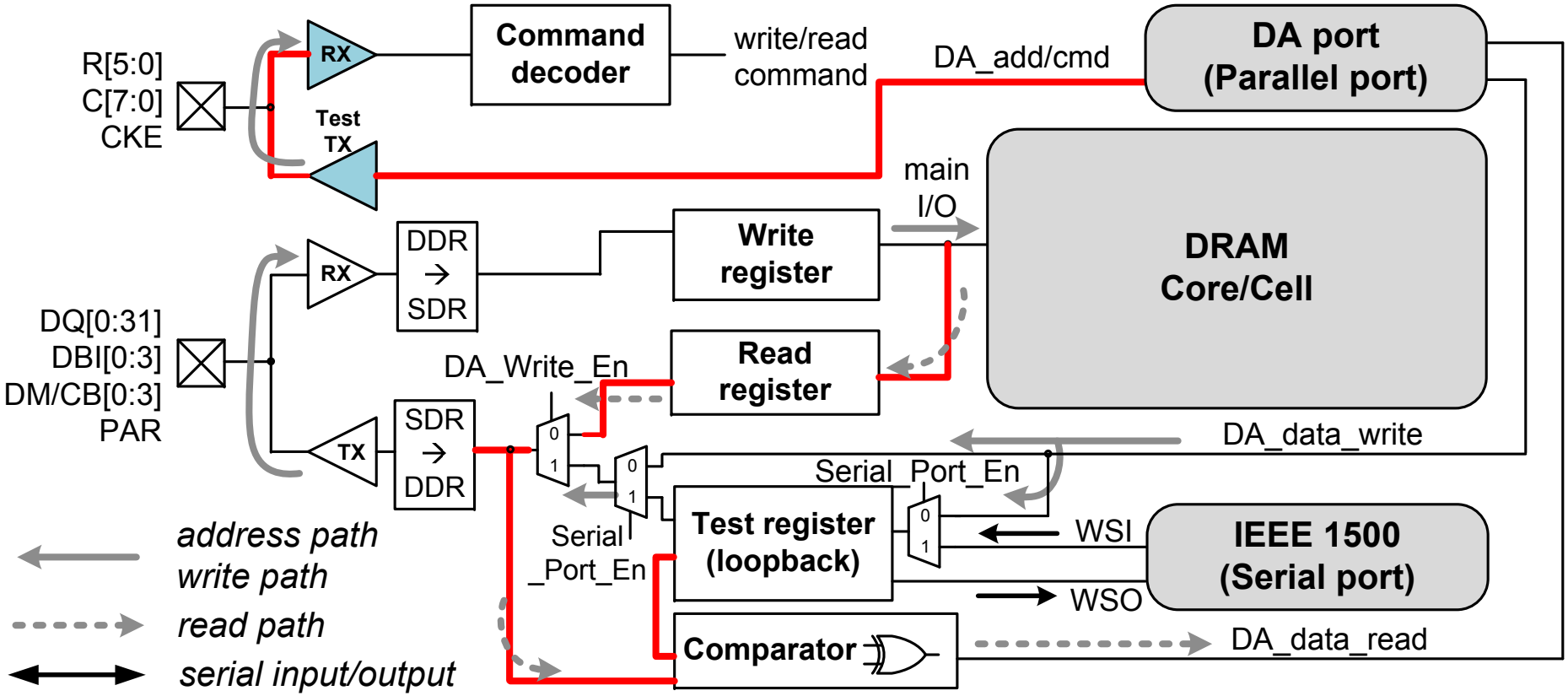
DA Port Test Method

- **PAD-loopback (address / write)**
  - TX and RX can be tested at the same time



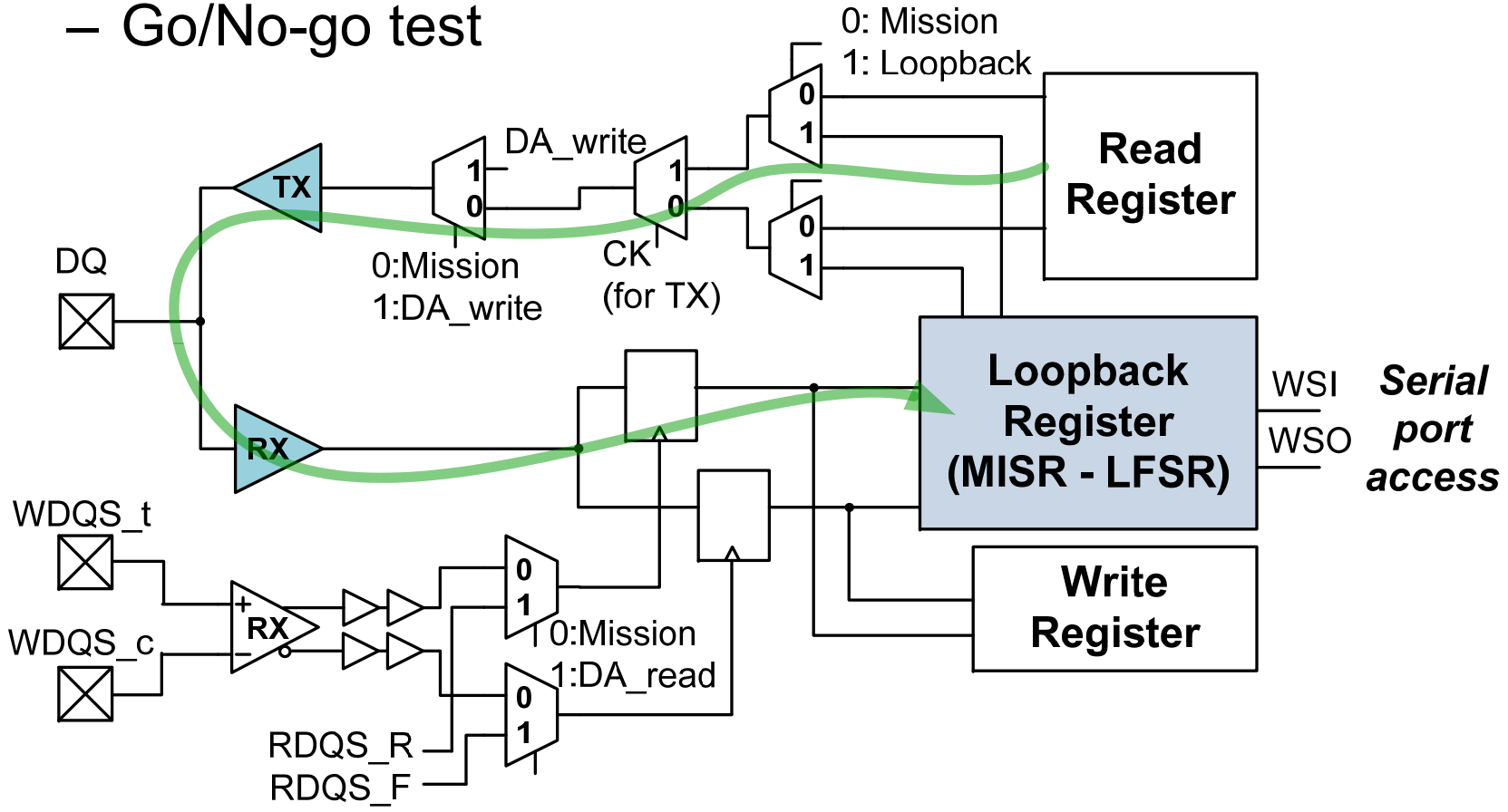
DA Port Test Method

- **Comparison with test register (address / read)**
  - High speed operation with increased fault coverage



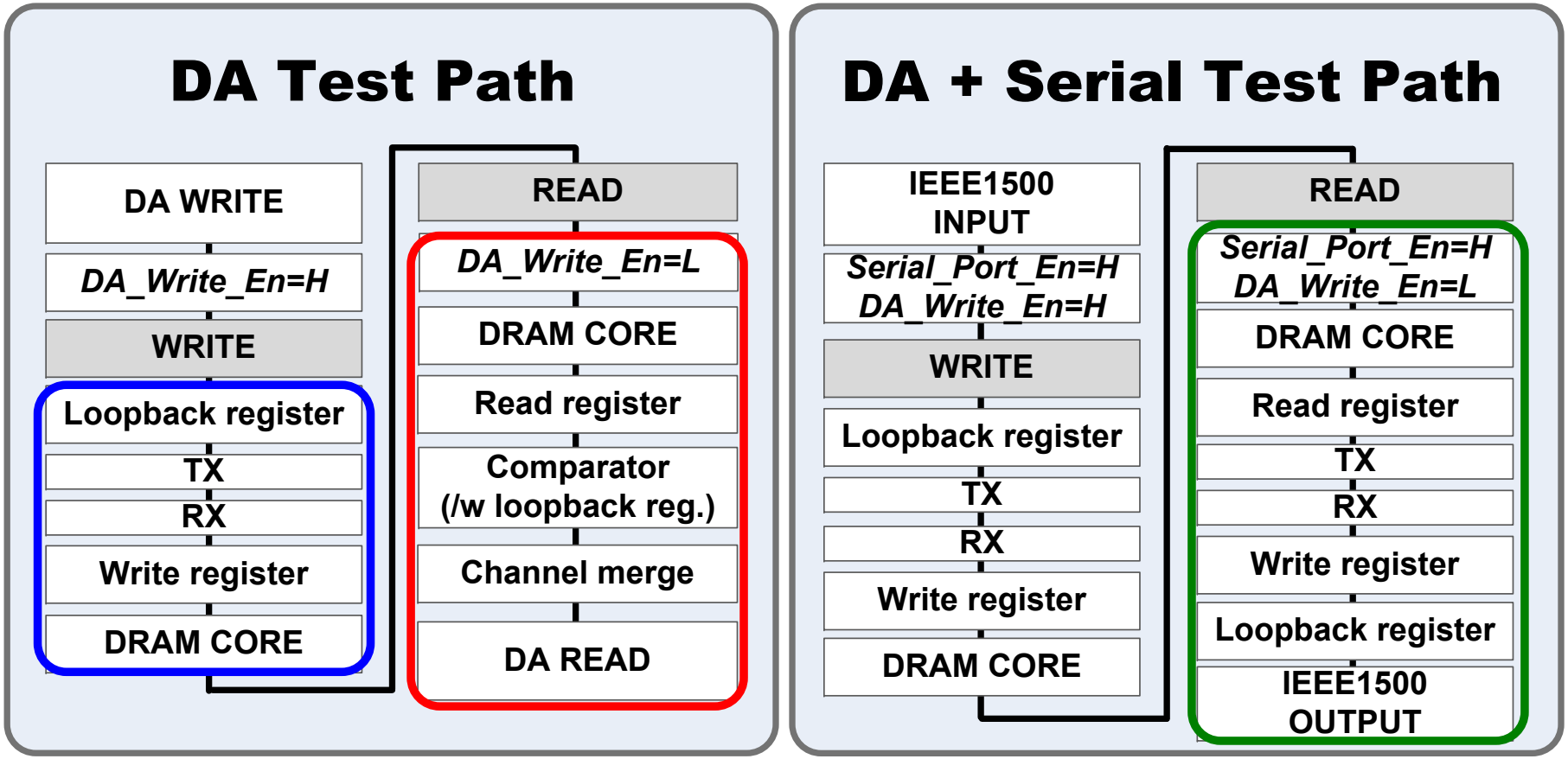
DA and Serial Port Test Method

- **TX / RX test while mission mode operation**
  - Read data compressed to loopback register
  - Go/No-go test



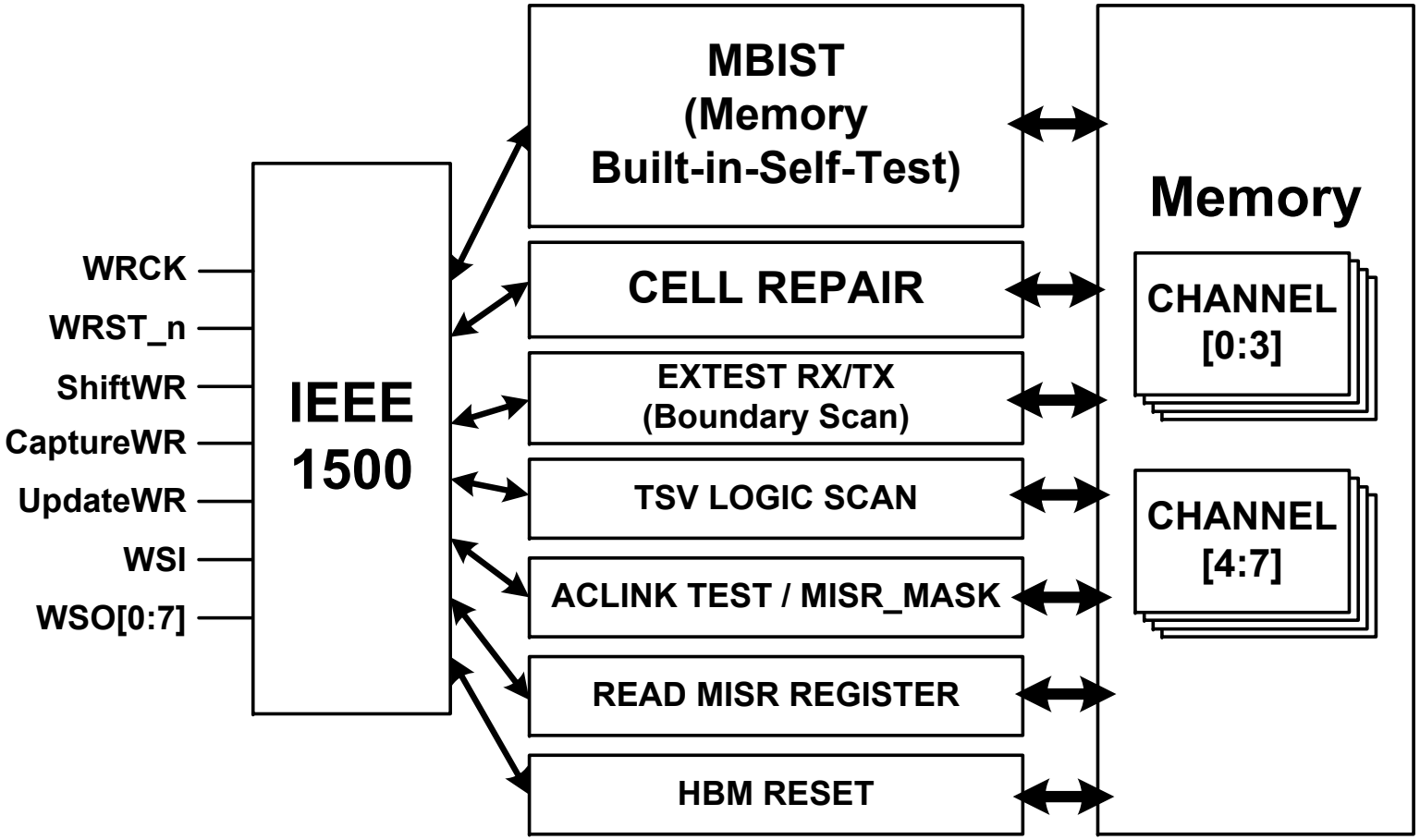
Microbump Test Path

- **Two way : DA path, DA+serial path**
  - Effective microbump test method



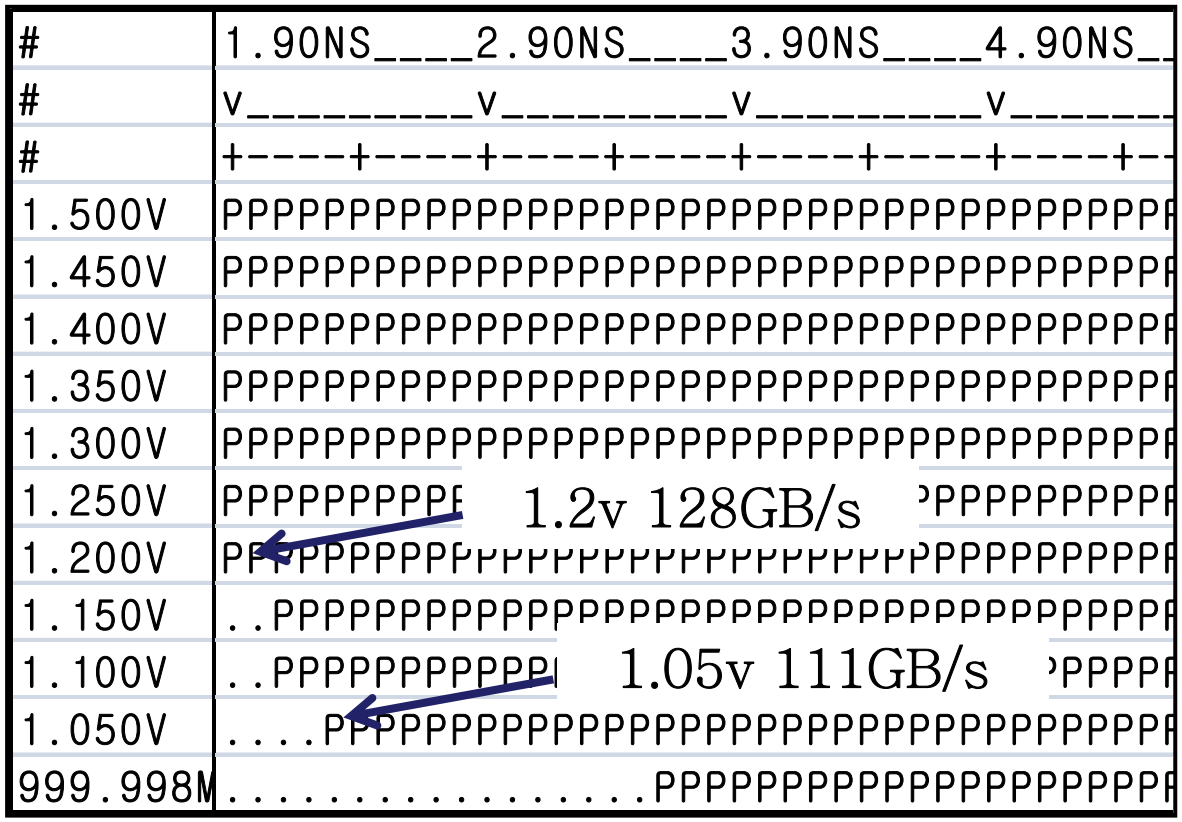
Serial Port Access Function

- **HBM DRAM test feature include test access port through IEEE 1500**



Shmoo Plot

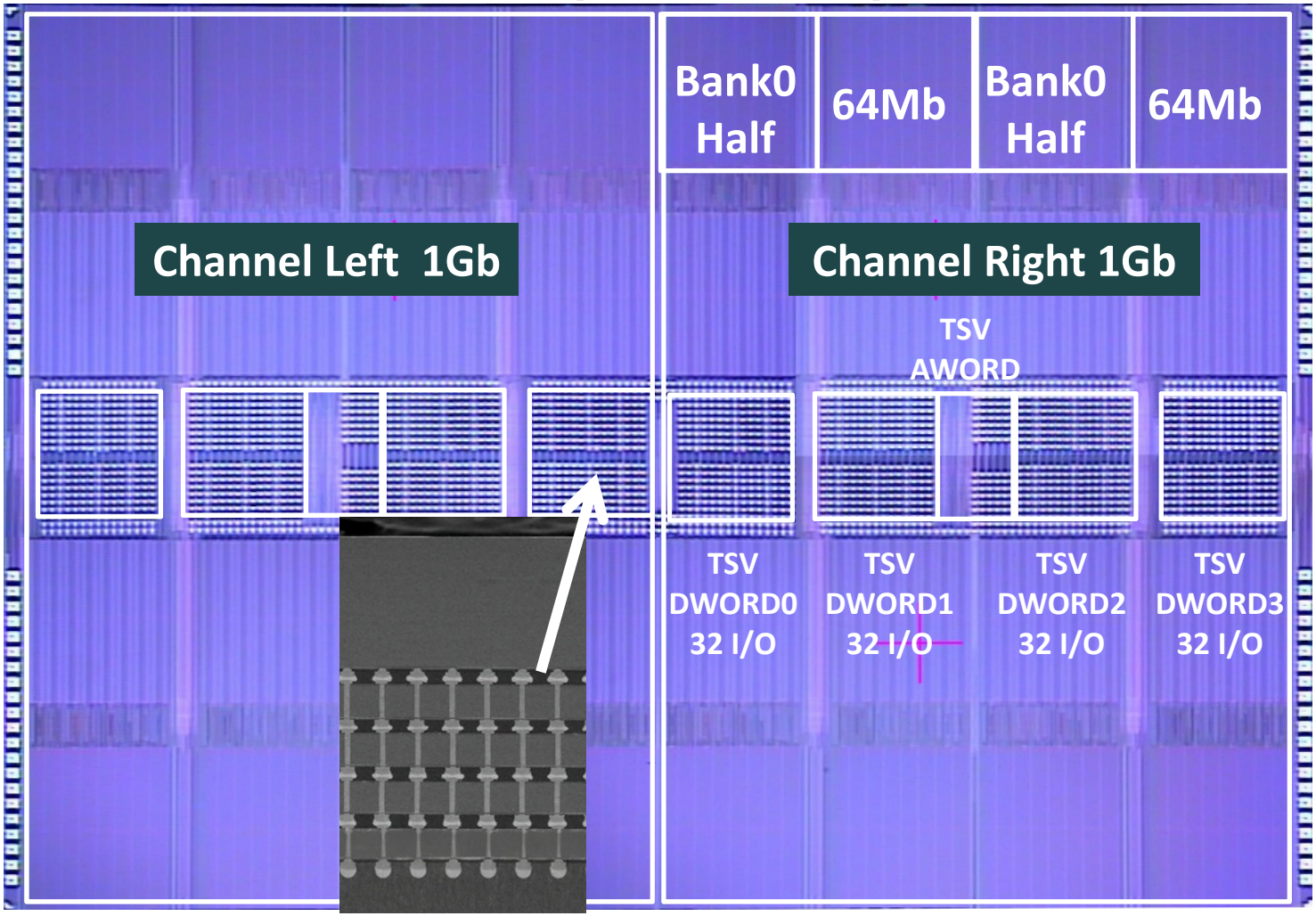
- **8-Ch seamless read operation (tCCD=2ns)**



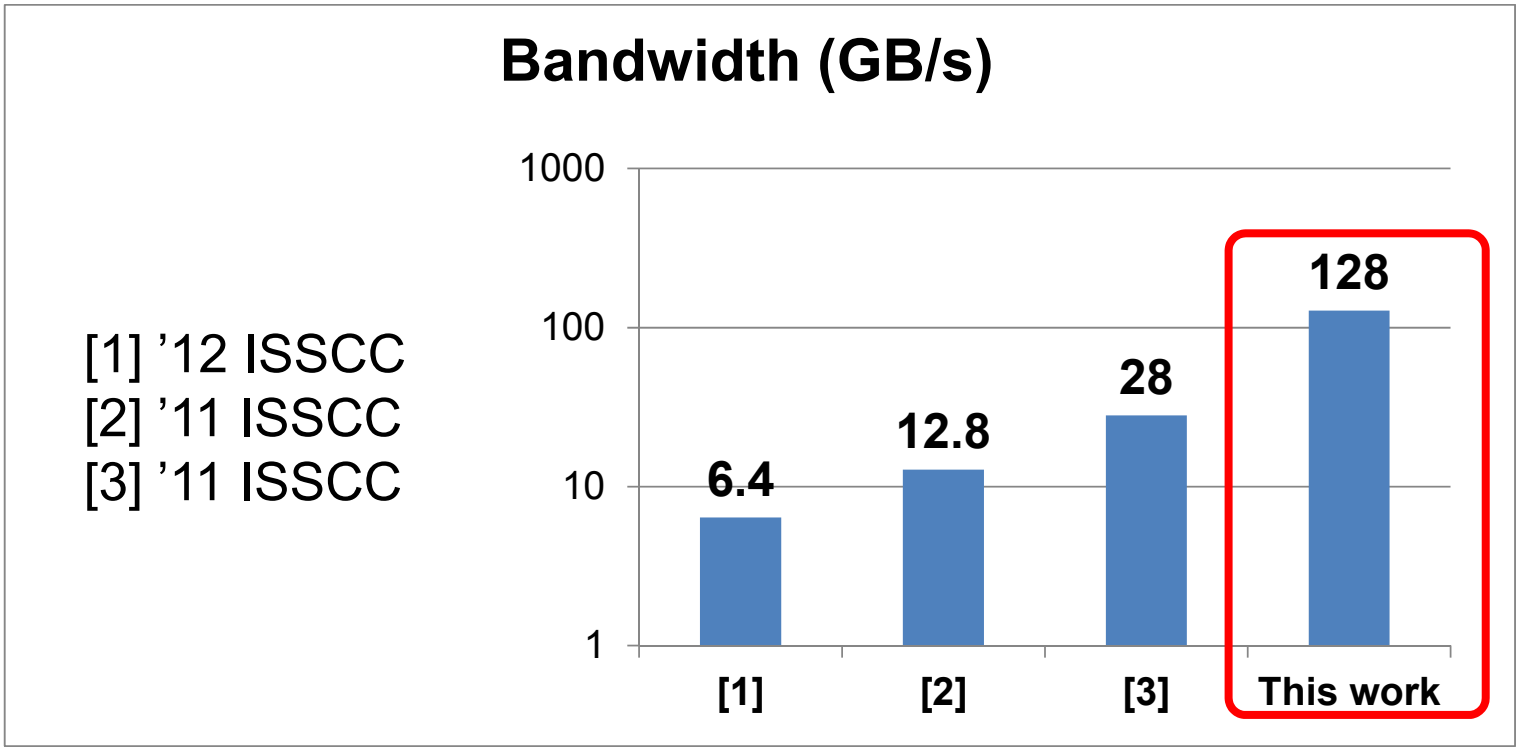
Process	29nm DRAM process
Chip Size	5.10mm x 6.91mm
Organization	8 bank x 8 channel x 128 I/O (total 1024 I/O)
Density	1Gb / channel
Microbump pitch (base die)	48 µm x 55 µm
Supply Voltage	VDD=1.2v, VPP=2.5v
Refresh	8k / 32ms
Page Size	2KB
Data Rate	1.0 Gbps (128GB/s)
C_{IO}	0.4pF

Chip Micrograph

- **Core : 2Gb DRAM (one slice)**



Chip Performance



Type	DDR4 [1]	WIO [2]	GDDR5 [3]	HBM
Total Density	4Gb	2Gb	2Gb	**8Gb**
Total IO width	16	512	32	**1024**
Total # of banks	16	16	16	**64**
Total # of channels	1	4	1	**8**
Supply voltage	1.2v	1.2v	1.5v	**1.2v**

Summary

- **HBM with 8Gb 1.2v 128GB/s Operation**
  - 5-Hi stacked-DRAM using chip-on-wafer process
- **High Performance**
  - Dual command interface
  - Single bank refresh with tRAS counter
- **Microbump Test Methods**
  - DA and IEEE1500 test interface
  - PAD-loopback
  - Impedance monitor

A 1.35V 5.0Gbp/s/pin GDDR5M with 5.4mW Standby Power and an Error-Adaptive Duty-Cycle Corrector

Hyun-Woo Lee[1,2], Junyoung Song[2], Sang-Ah Hyun[1], Seunggeun Baek[1], Yuri Lim[1], Junghwan Lee[1], Minsu Park[1], Haerang Choi[1], Changkyu Choi[1], Jinyoup Cha[1], **Jaeil Kim[1]**, Hoon Choi[1], Seungwook Kwack[1], Yonggu Kang[1], Jongsam Kim[1], Junghoon Park[1], Jonghwan Kim[1], Jinhee Cho[1], Chulwoo Kim[2], Yunsaing Kim[1], Jaejin Lee[1], and Byongtae Chung[1]

[1]SK Hynix Semiconductor Inc.
[2]Korea University

Contents

- Motivation
- Functions & features
  - Chip architecture
  - Clocking system
  - Auto sync. mode
  - EA-DCC
- Implementation and measurement results
- Conclusion

Motivation

High performance target & general-purpose product
➔ Background of GDDR5M

DDR3: Commodity memory

- General-purpose product
- (JEDEC standard)
- Low cost(price-sensitive)
- Low performance

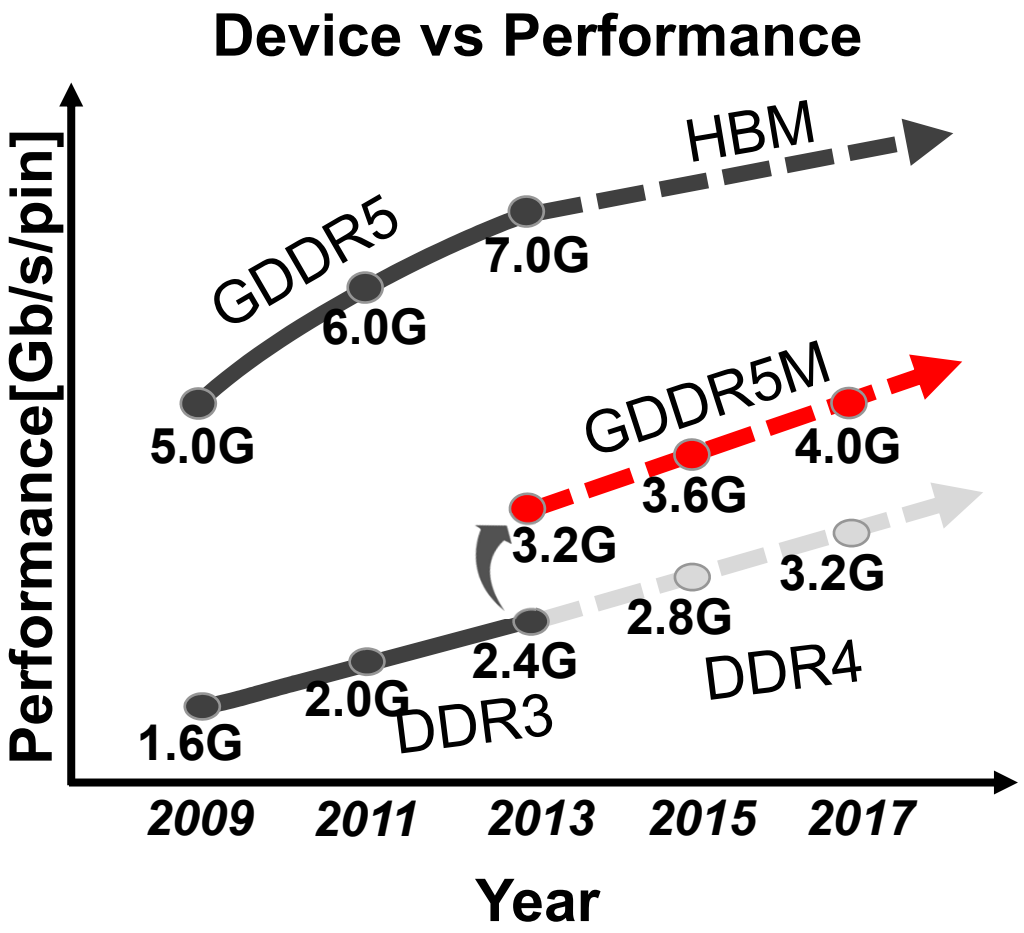
GDDR5: Graphics memory

- Only for graphics
- Cost penalty
- High-performance product

Cost : 5~10% higher than DDR3

Speed : 3.2~4.0Gbps @ 1.35V

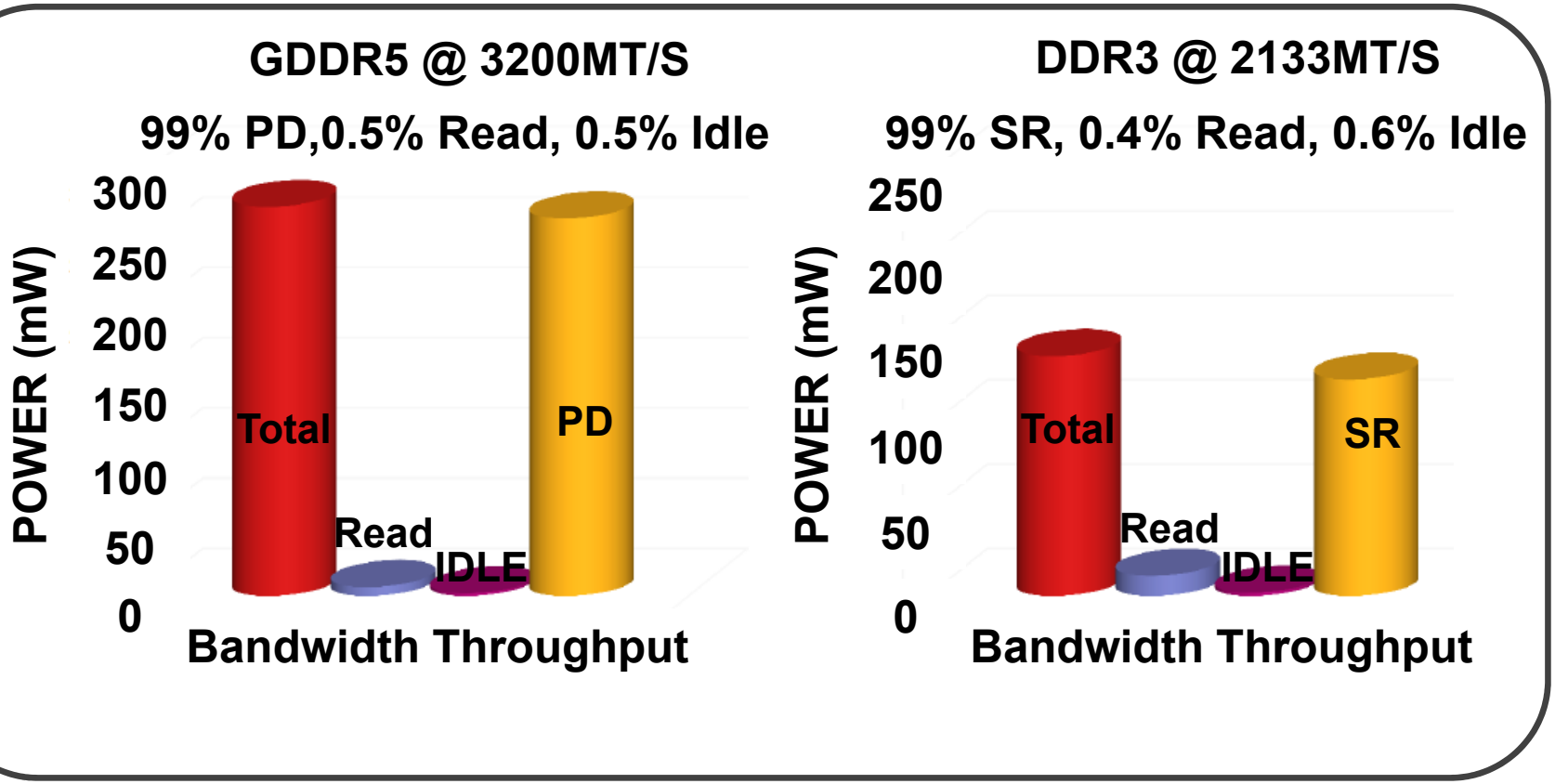
Motivation



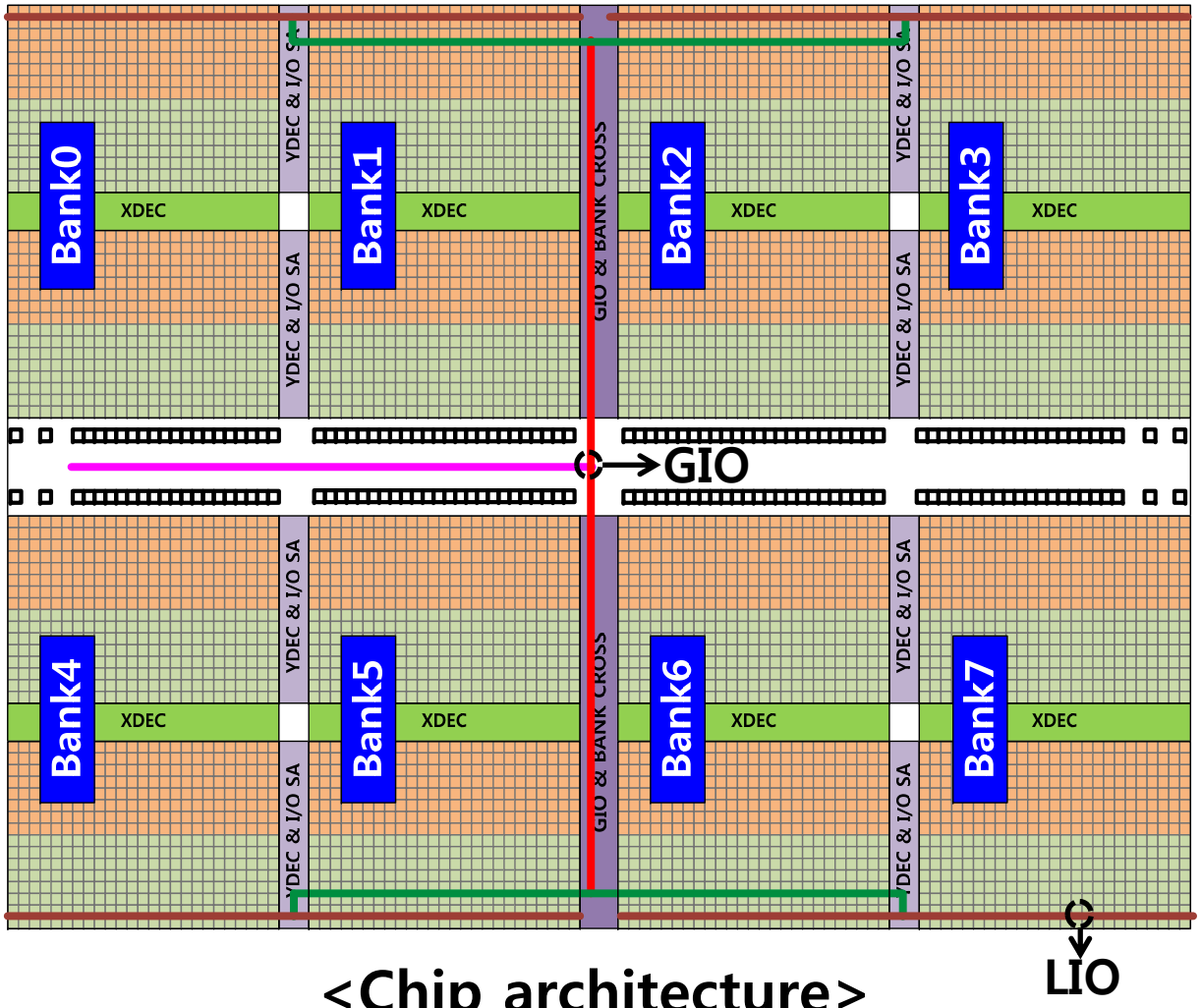
- The mid-range product between GDDR5 and DDR3
- High performance compared to DDR3
- More cost-effective than GDDR5

Power Requirement

- DDR3(64bit & 99% Self Ref.) vs GDDR5(32bit & 99% PD mode)
- Standby power : Need to achieve; IDD6@DDR3 = IDD2P0@GDDR5



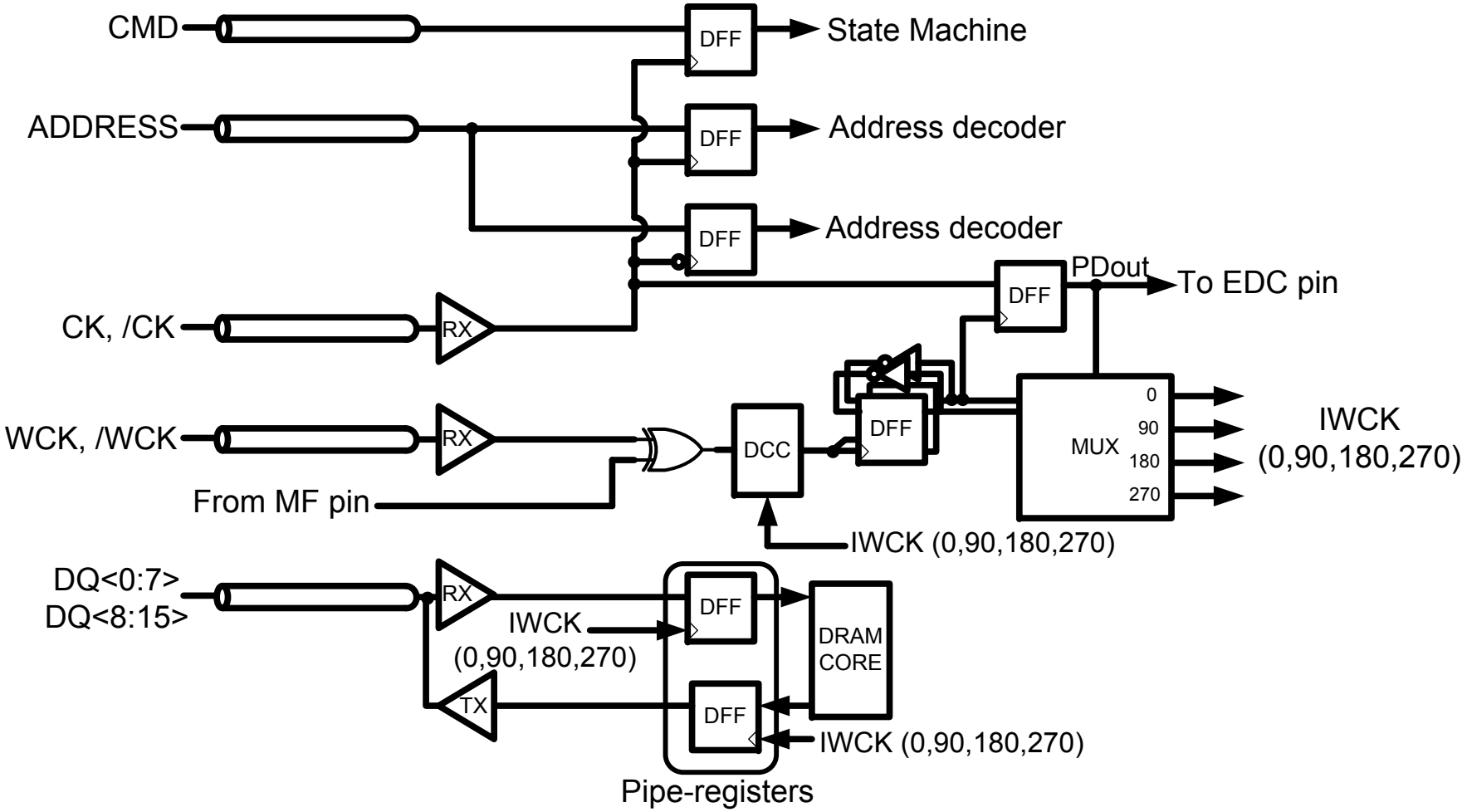
Chip Architecture



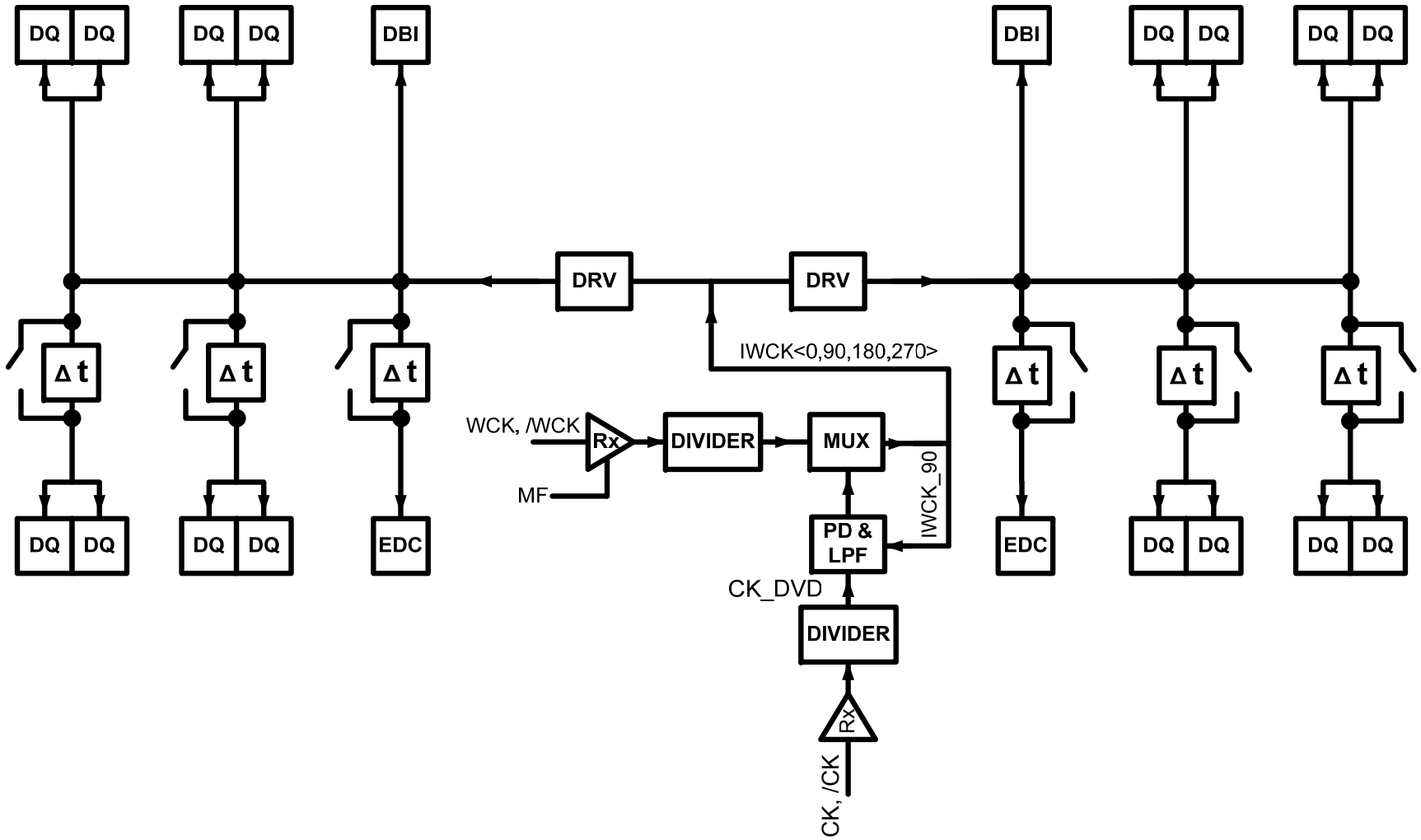
<Chip architecture>

- LIO/GIO symmetric structure
- Minimize skew by BANK
- Minimize YI & LIO length

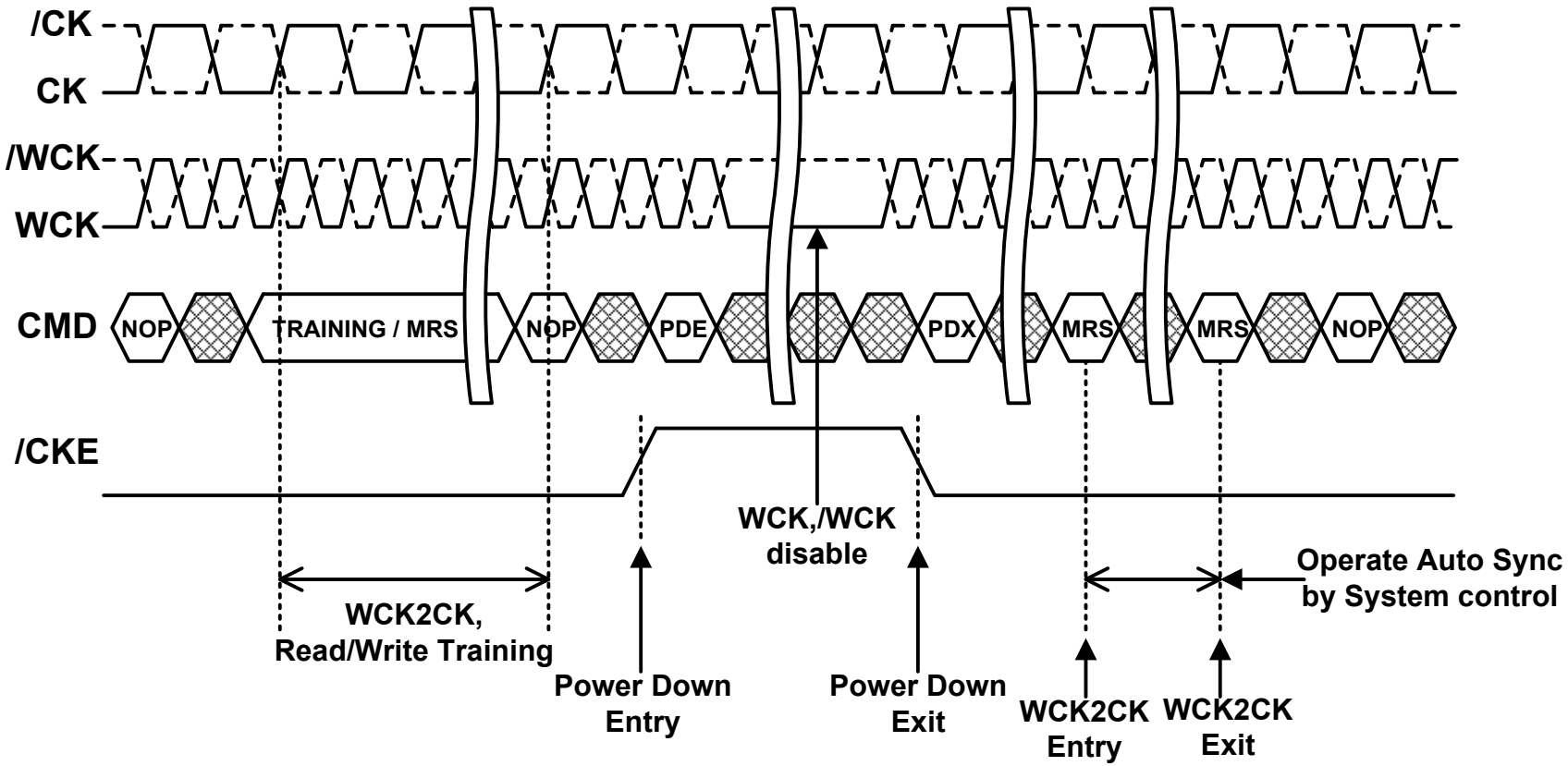
Clocking System



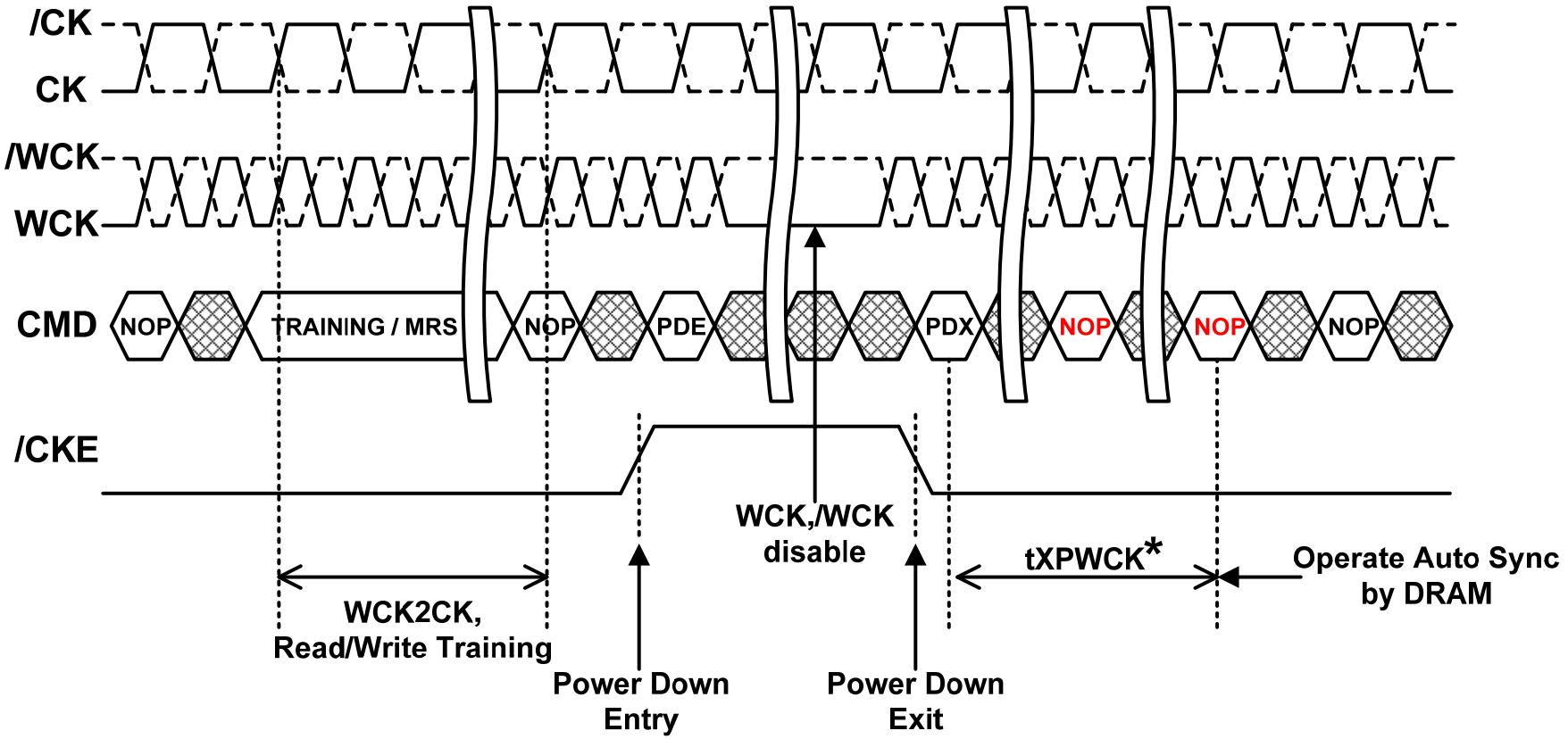
Clock Tree



Auto-Sync Mode in GDDR5

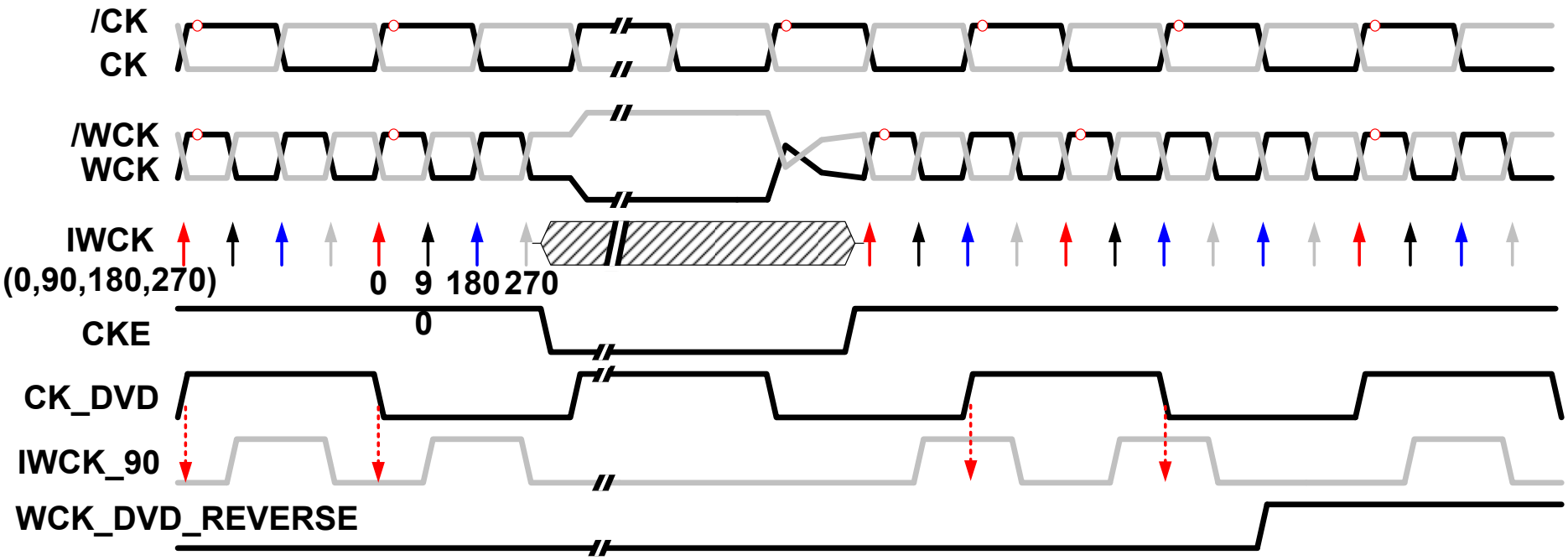


Auto-Sync Mode in GDDR5M



tXPWCK* : Power-down exit time for commands requiring WCK

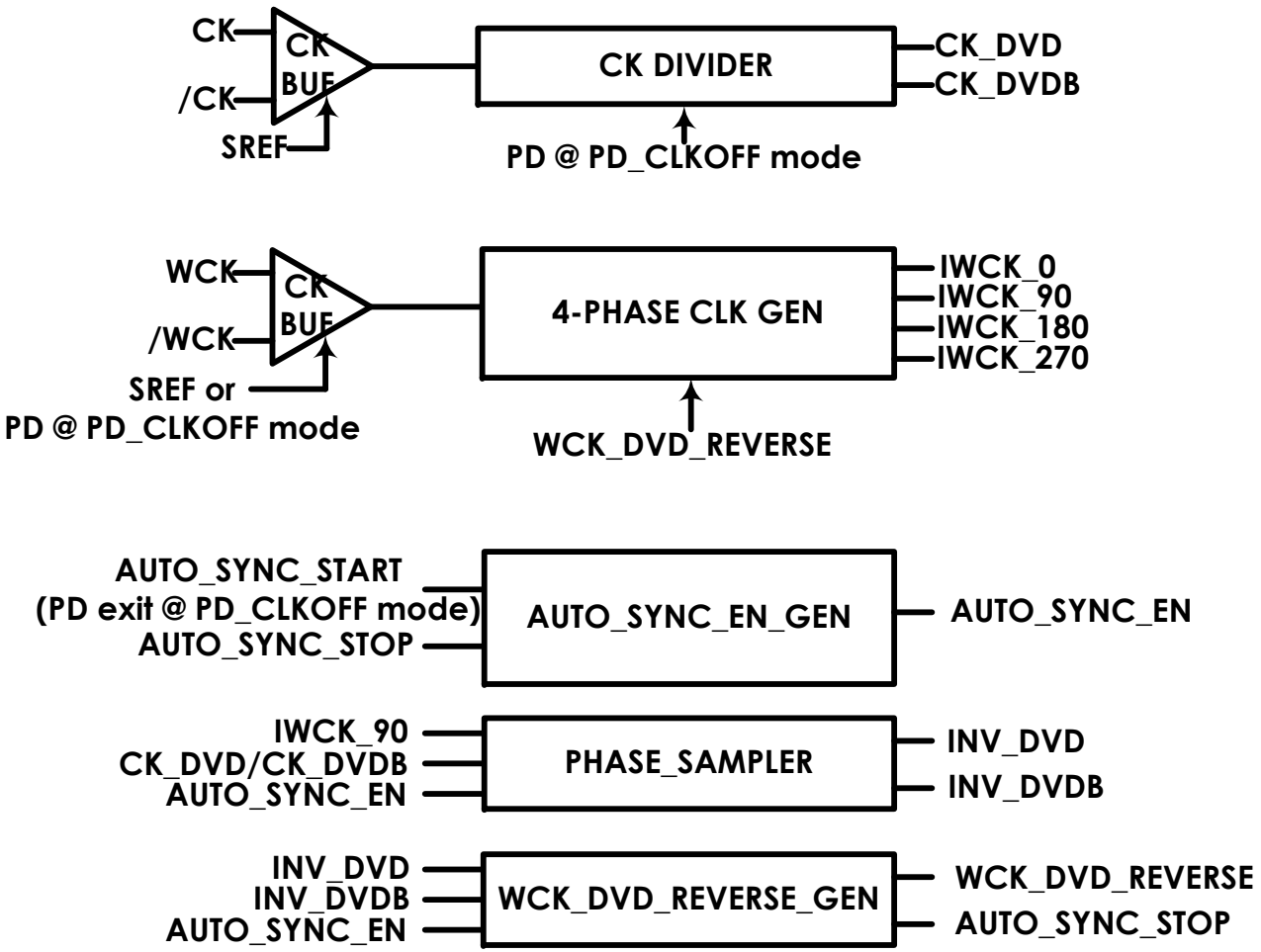
Auto-Sync Mode



<Timing diagram of auto-sync with WCK stop mode>

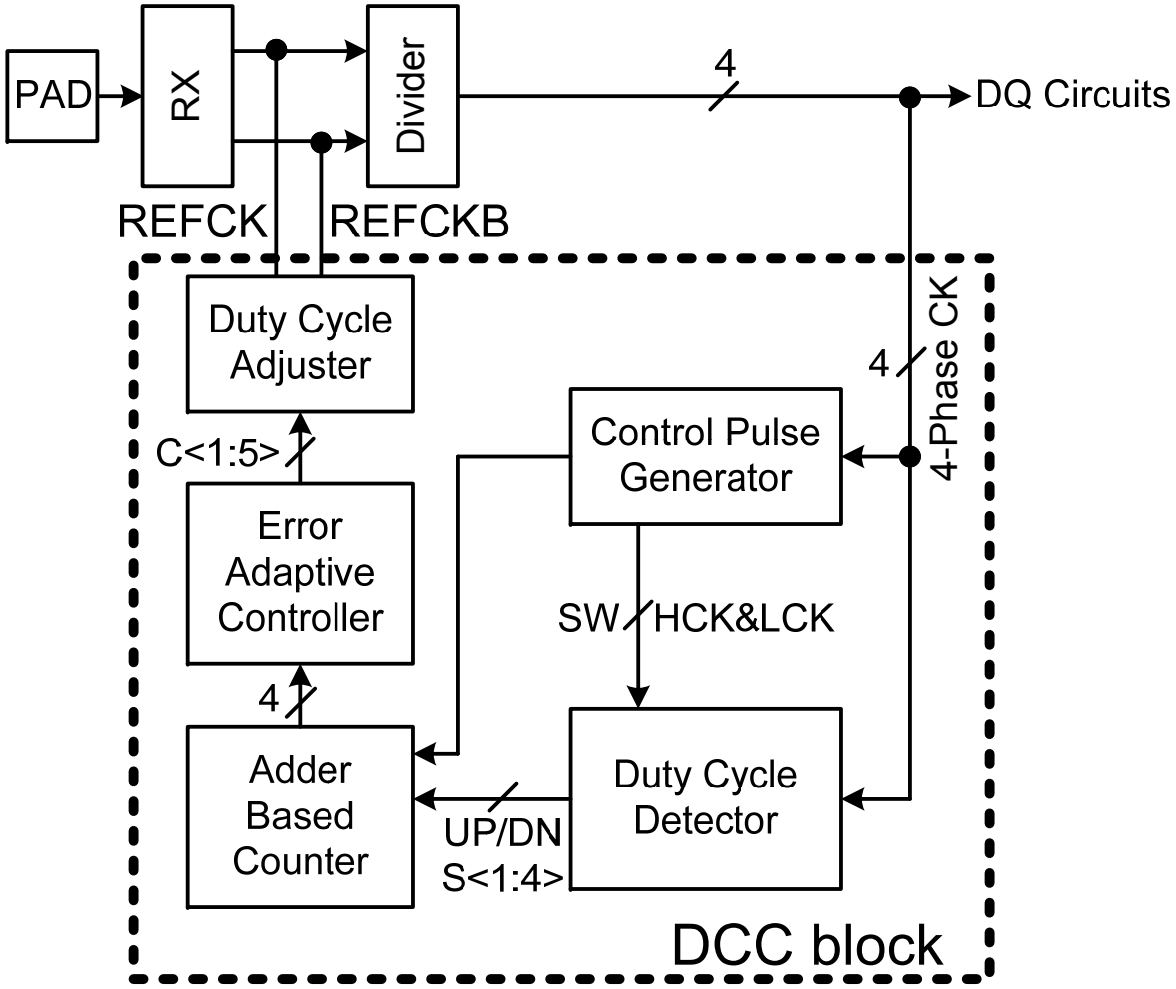
- CK_DVD is low ➔ WCK_DVD_REVERSE stays low
- CK_DVD is high ➔ WCK_DVD_REVERSE goes to high

Auto-Sync Mode



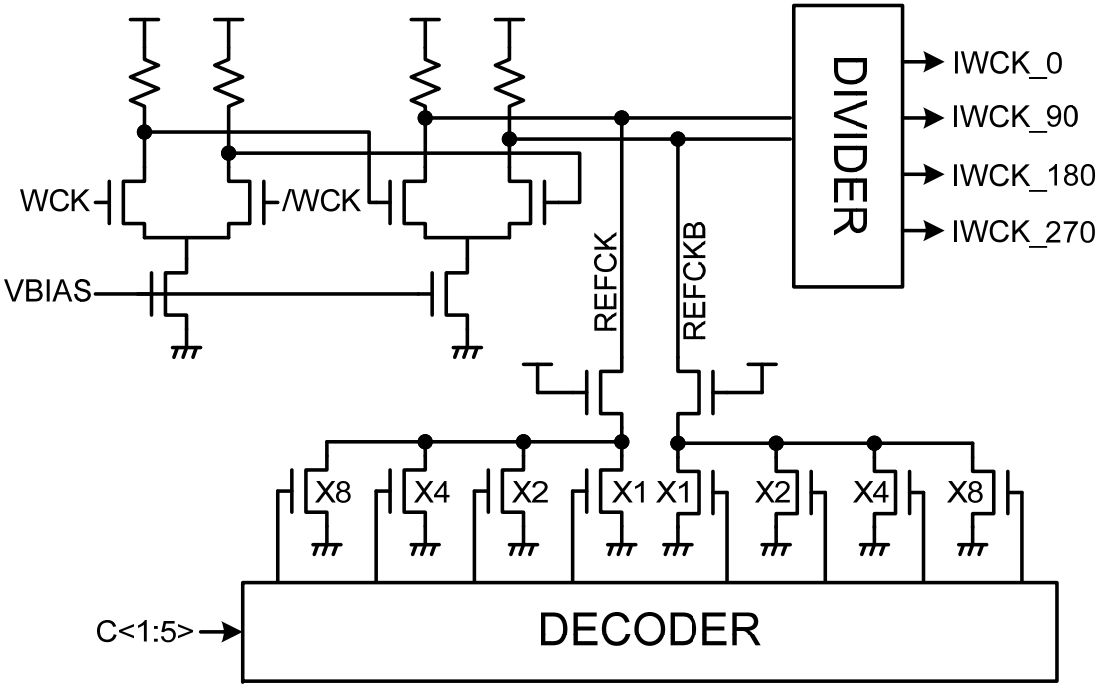
<Block diagram of auto-sync mode circuit>

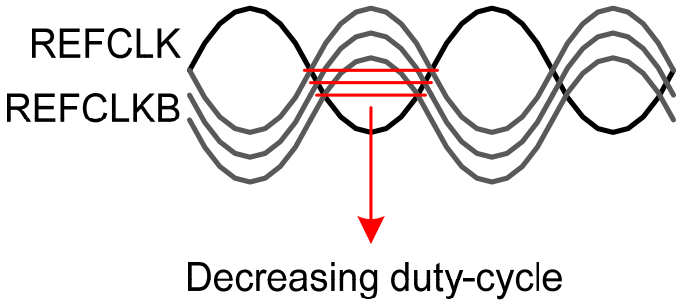
Error Adaptive DCC



<Clock distribution path with DCC in GDDR5M>

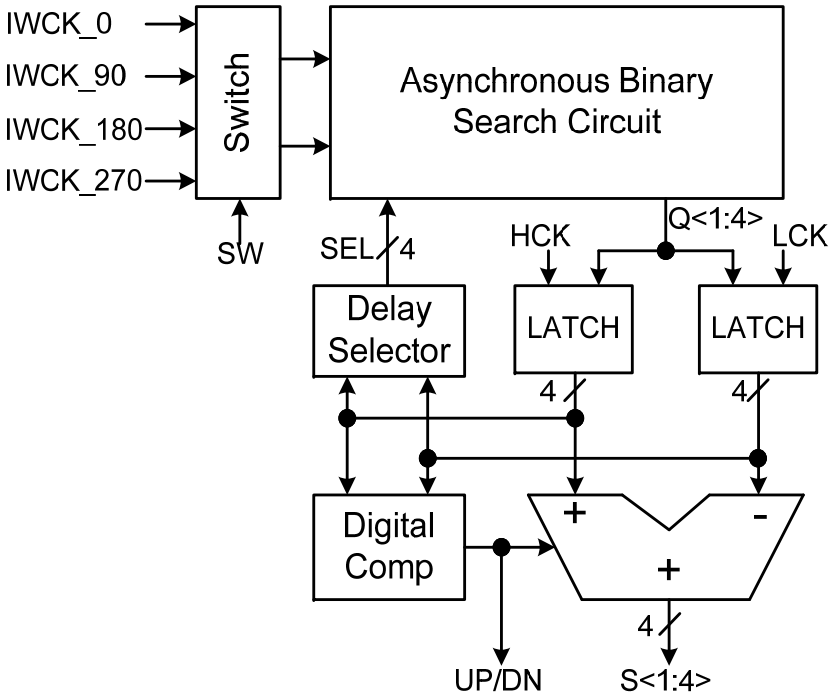
Error Adaptive DCC

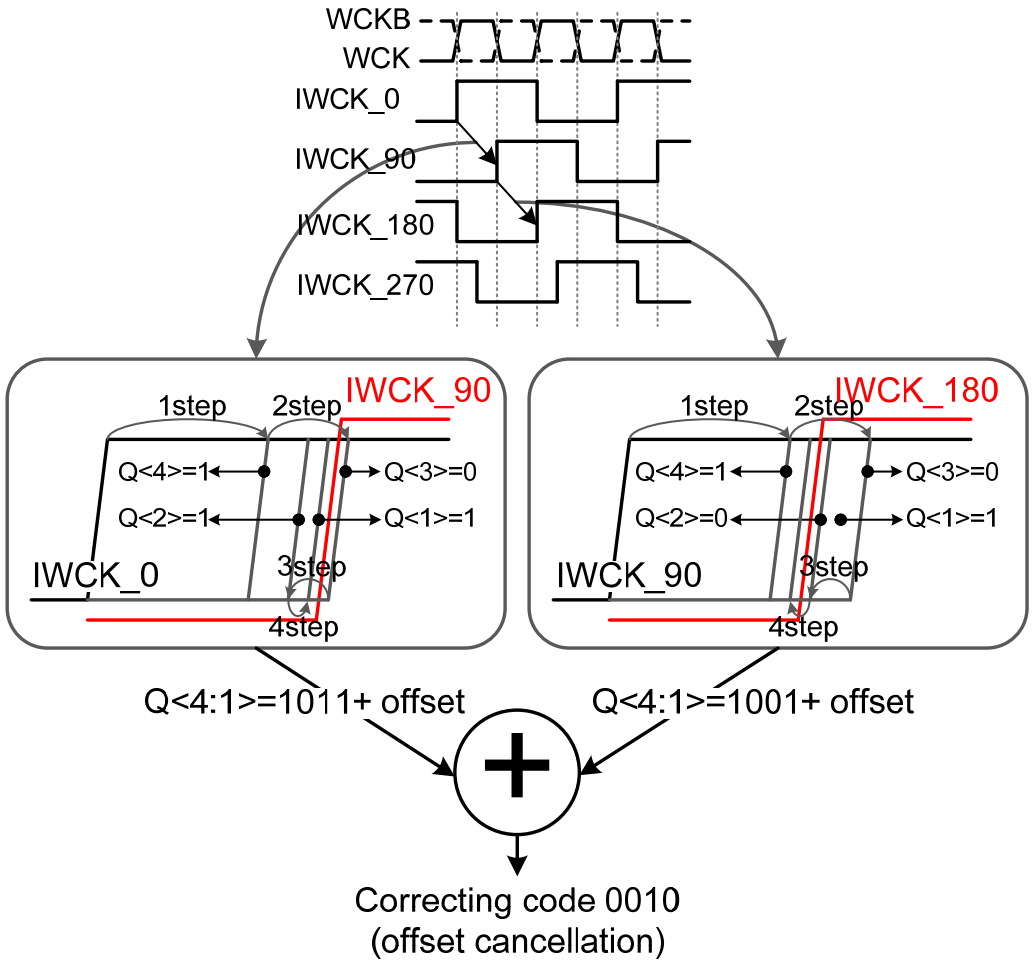




<Duty cycle adjuster>

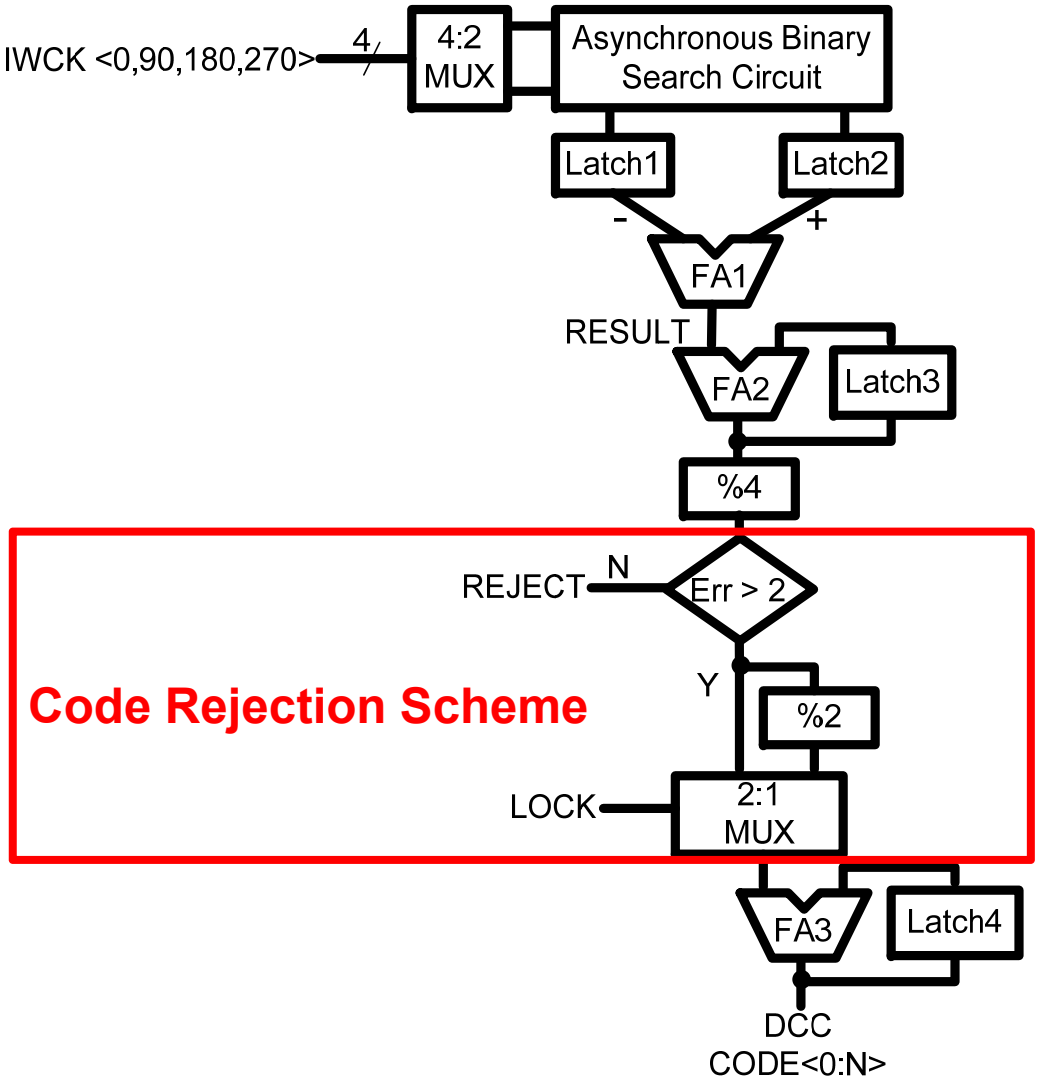
Error Adaptive DCC





<Duty cycle detector>

Error Adaptive DCC



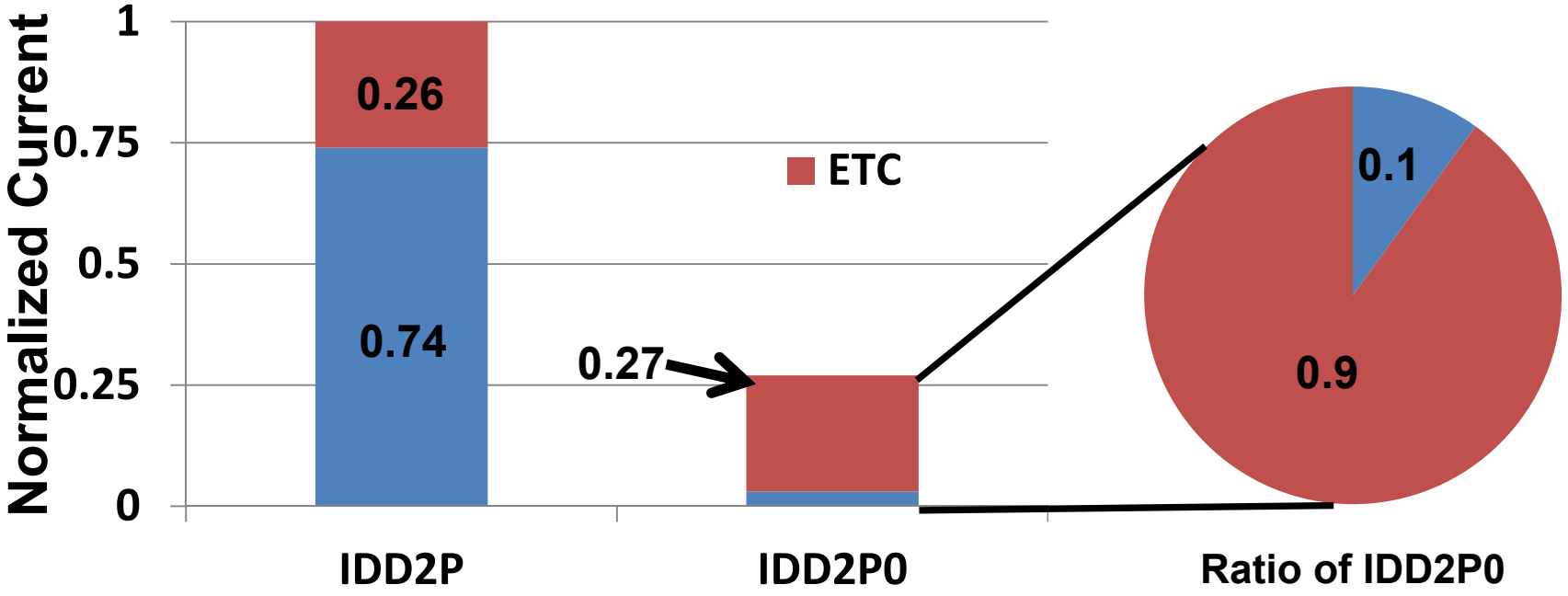
Chip Summary

Item	DDR3	GDDR5	GDDR5M
Data Rate (Per Pin)	~2.1Gbps	~8Gbps	~5Gbps
I/O Organization	X4 / X8/ X16	X16 / X32	X8 / X16
CA / DQ Bus	SDR / DDR	DDR / QDR*	DDR / QDR*
Interface	CTT	POD	POD
DQ Termination	Supported (1/2 VDD)	Supported (VDDQ)	Supported (VDDQ)
Voltage	1.5V	1.5V	1.35V
Auto-sync	-	Auto-sync mode by System	Auto-sync mode by DRAM

<GDDR5M vs. DDR3&GDDR5>

QDR* : QDR to CK

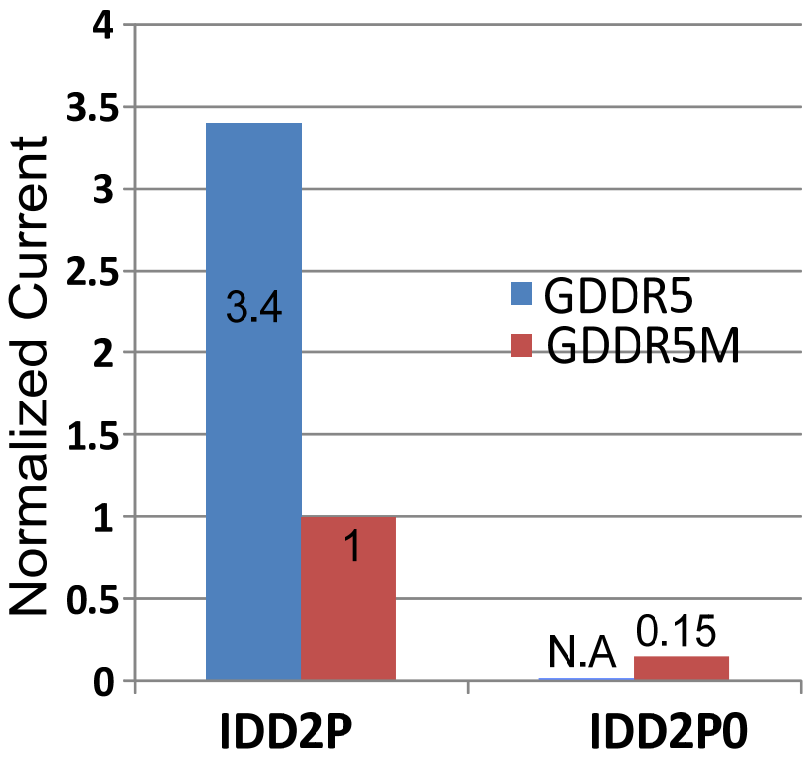
Simulation Results

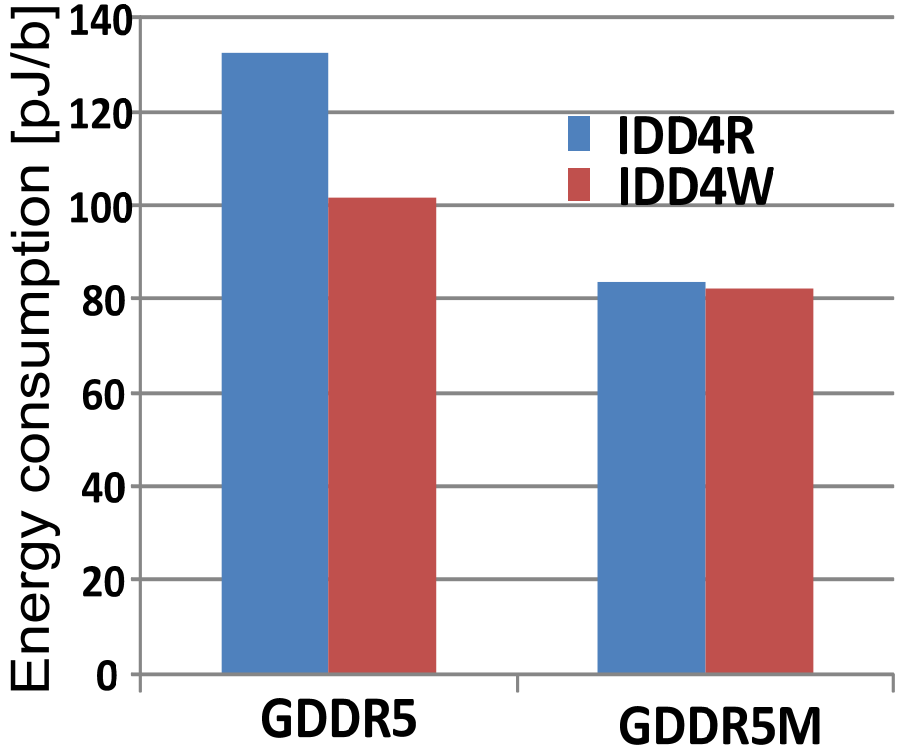


CDN* : Clock distribution network

<CDN current consumption of GDDR5M @ power down mode >

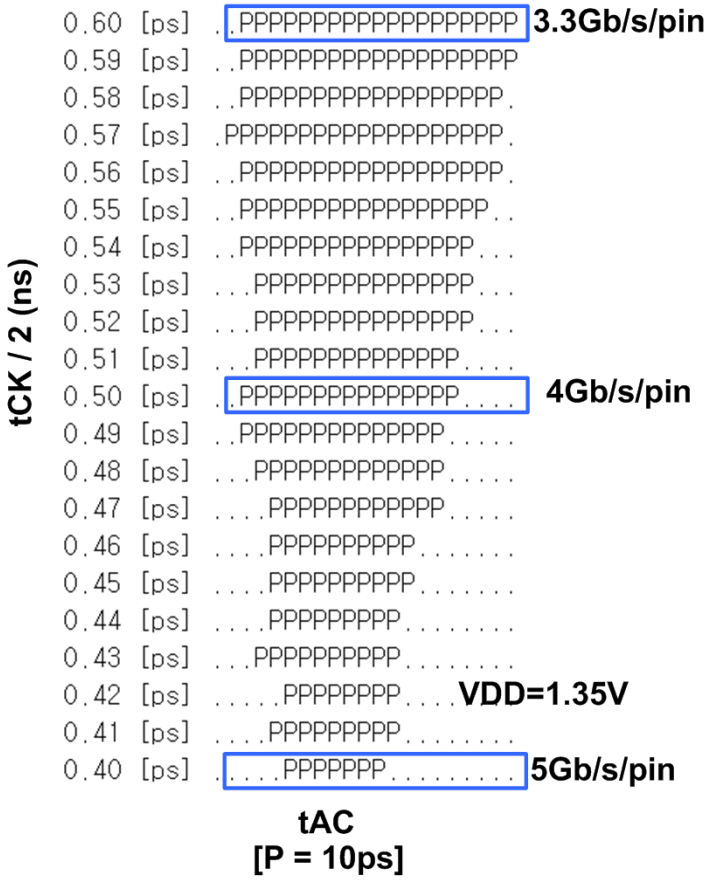
Measurement Results





<Power consumption comparison between GDDR5 and GDDR5M>

Measurement Results



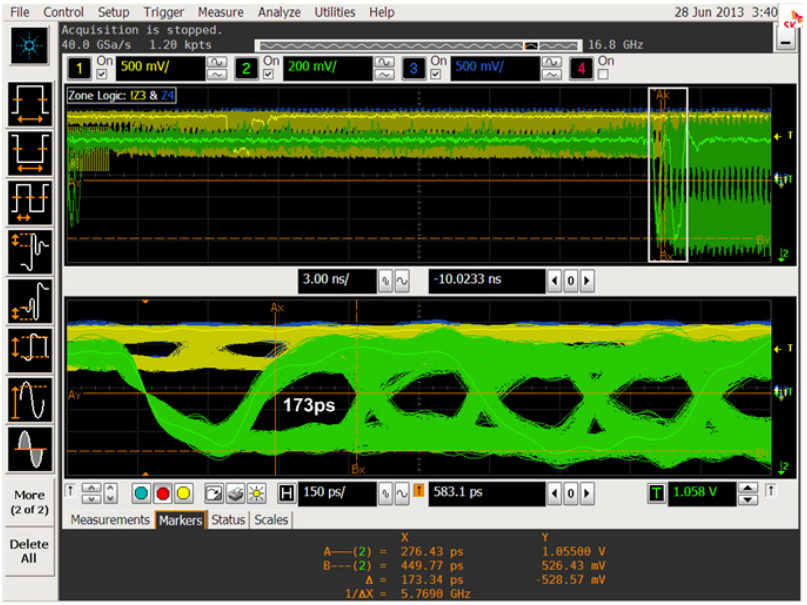
<Shmoo plot of tCK-tAC at 1.35V>

Shmoo plot of tCK vs. tAC				tDV [ps]	
Previous		Proposed		Previous	Proposed
tCK / 2 (ns)	0.55 [ps] ..PPPPPPPPPPPPPPP...	tCK / 2 (ns)	0.55 [ps] ..PPPPPPPPPPPPPPP..	150	160
	0.54 [ps] ..PPPPPPPPPPPPPPP...		0.54 [ps] ..PPPPPPPPPPPPPPP..	150	160
	0.53 [ps] ...PPPPPPPPPPPPP....		0.53 [ps] ..PPPPPPPPPPPPPP...	130	150
	0.52 [ps] ...PPPPPPPPPPPP.....		0.52 [ps] .PPPPPPPPPPPPPP....	120	150
	0.51 [ps] ...PPPPPPPPPPPP....		0.51 [ps] .PPPPPPPPPPPPPP.....	130	140
	0.50 [ps] ..PPPPPPPPPPPPP.....		0.50 [ps] ..PPPPPPPPPPPPP.....	130	130

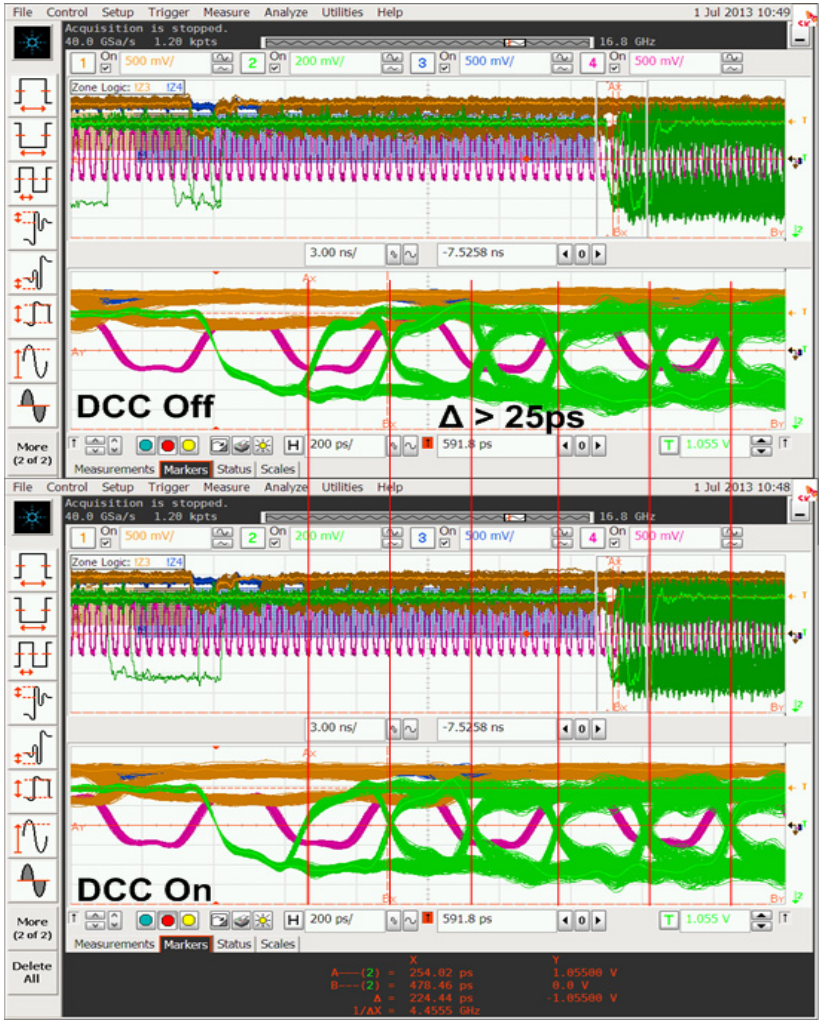
<Shmoo plot of tCK-tAC at 1.4V with proposed clocking scheme>

- Operating speed :5Gbps@ 1.35V
- tAC window : 70ps
- tDV is widened by adding timing skew to lower DQs

Measurement Results



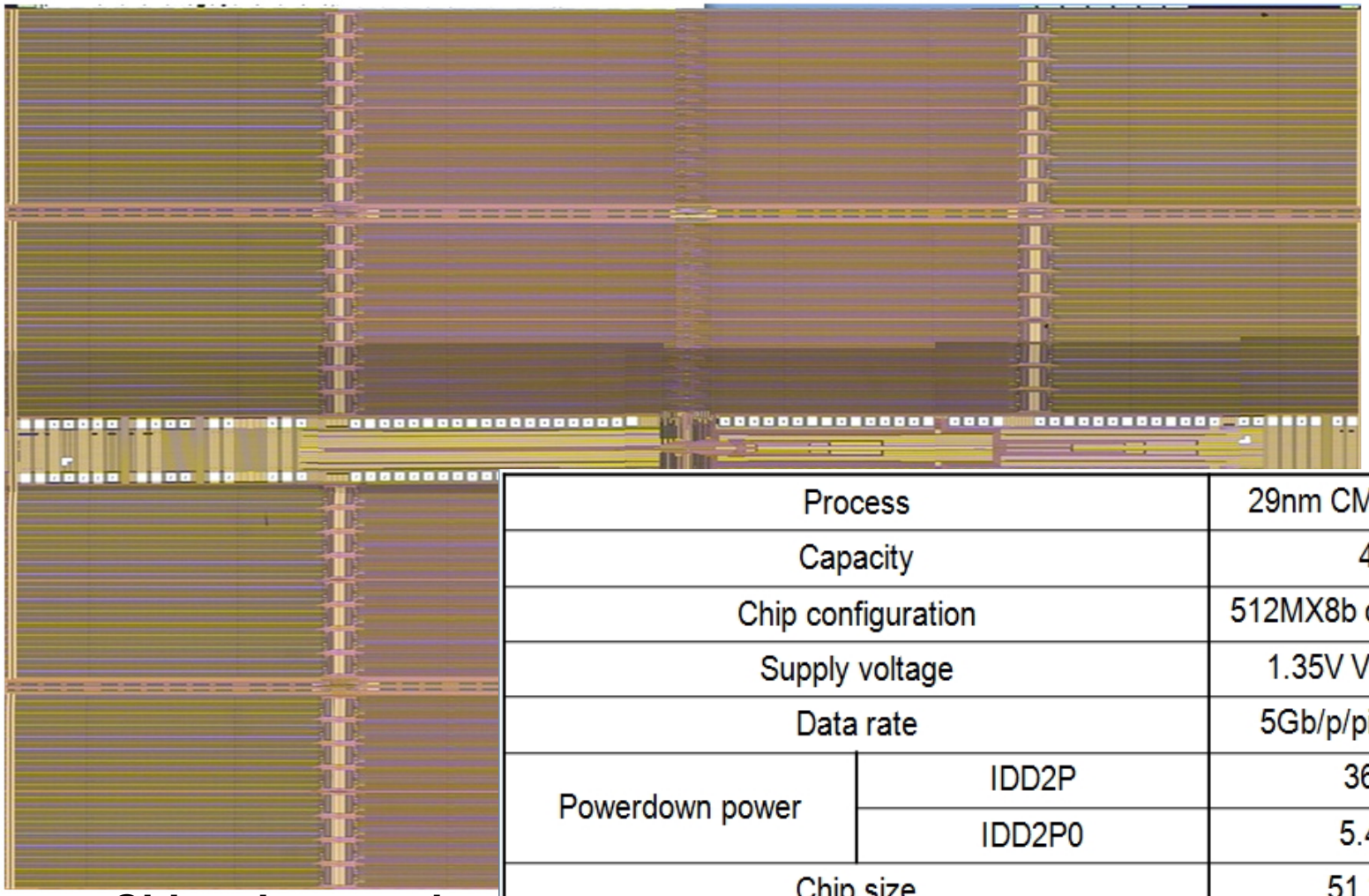
<DQ6 with worst pattern>



<With 3% distorted WCK at 4.2Gb/s in graphics card>

- **EA-DCC corrects the duty error**

Implementation



<Chip micrograph>

Process		29nm CMOS 3 metal
Capacity		4Gb
Chip configuration		512MX8b or 256MX16b
Supply voltage		1.35V VDD/VDDQ
Data rate		5Gb/p/pin @ 1.35V
Powerdown power	IDD2P	36mW
	IDD2P0	5.4mW
Chip size		51.2mm^2

<Chip summary>

Conclusion

- A 5Gb/s/pin GDDR5M is implemented in a 29nm CMOS 3-metal process

- GDDR5M is an effective solution as respect to power consumption and performance
  - IDD2P0 minimization with auto-sync mode
  - Lower VDD/VDDQ compared to DDR3/GDDR5
  - Operating speed of 5Gbps@1.35V

- Implemented GDDR5M has the following features
  - Auto-sync mode by DRAM
  - SSN minimization by adding timing skew to the lower DQ
  - Optimized duty cycle by using EA-DCC